ROCSTAR: Data Acquisition Electronics for TOF PET

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I. Introduction

A high spatial resolution, time-of-flight scanner is currently being developed at the University of Pennsylvania [1]. This instrument is targeted for breast imaging, though it is general enough to be adapted for other applications. The detector design is modular, each module consisting of a single Hamamatsu H8500 multi-anode (MA) PMT coupled to a 32x32 array of LYSO crystals, which can be tiled in any desired configuration. For the breast scanner (bPET) we are constructing two detectors, each with 6-8 modules. Instrumenting this scanner requires a data acquisition system that combines excellent timing resolution, high countrate capability, and scalability – a combination that was not easily found in currently available systems. This paper reports on the development of custom data acquisition electronics to fill this need, called ROCSTAR (ROw Column Summing Timing And Readout). While the data acquisition system is being developed specifically for this detector, it is sufficiently general that it could be used in any application utilizing an 8x8 array of sensors, where row-column summing is appropriate and a highly accurate timing measurement is desired. The electronics architecture will be presented, along with simulations to determine the relevant specifications. Measured results with the prototype electronics and progress toward the production of a complete board will also be presented.

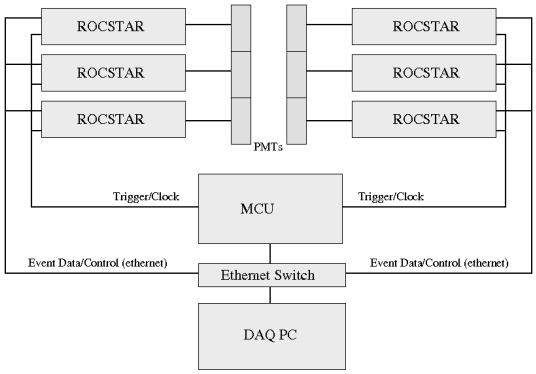

Fig. 1. bPET electronics system block diagram. Each PMT is read out by a single ROCSTAR board. The MCU (center) controls both coincidence logic and clock distribution. Event data and control signals travel over ethernet.

II. Electronics Architecture

The PET detector design is modular with one MA-PMT (coupled to a crystal array) forming the basic unit which can be tiled in any desired configuration. This electronics design follows that modularity, with one ROCSTAR board serving one PMT and the trigger logic being digitally reconfigurable. Block diagrams of the electronics architecture can be seen in Figs. 1 and 2. The design of this data acquisition system borrows heavily from the work done by this group on our whole-body LaPET scanner [2], most notably in the usage of the DRS4 chip for the timing measurement and in the trigger design.

The event position (crystal ID) is determined by the 64 anodes. A prominent feature of the ROCSTAR design is the use of row-column summing to reduce the number of readout channels. Prior to beginning the ROCSTAR electronics design, simulations were run and a prototype was built to determine and verify that row-column summing did not degrade the quality of the floodmap. These tests were reported in [1] and showed excellent crystal discrimination, even extending out to the edges of the array (fig. 3). The anode signal chain is constructed as follows: Each anode signal first passes through a variable gain amplifier, which will allow for cancelling of PMT gain variations. Next the rows and columns are summed together, reducing the channel count from 64 to 16. The signals are then shaped for sampling and integration before being sampled at 100 Msps with a resolution of 12 bits. The summed anode signals are digitally integrated in firmware in real-time by a simple sum of the previous N samples. This system provides a simple charge integration measurement with zero dead-time and can provide very high resolution, provided that the signal is properly shaped and the ADC has sufficient speed and resolution. Position calculations are performed using the integrated charge in the row-column sum signals and a weighted centroid algorithm.

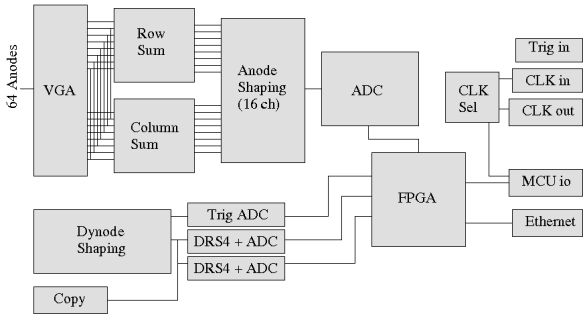

Fig. 2. Block diagram of ROCSTAR board.

The common dynode output is used for measuring both event timing and energy. The dynode signal will be moderately shaped with tail cancellation and digitized at a rate of up to 5 Gsps using the DRS4 chip from PSI [3]. The timing and energy information will be extracted digitally from the

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sampled waveform. Waveform sampling provides a number of advantages such as a flexible definition of the timing pickoff, which allows us to optimize the timing measurement across the face of the PMT. This flexibility, along with the added waveform information, also allows us to compensate for factors degrading the timing resolution at high rates, such as pile-up.

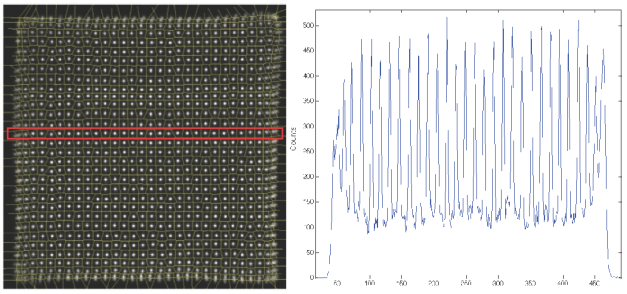

Fig. 3. Left: Floodmap with the full 32x32 crystal array using prototype row-column summing readout. Right: A profile (indicated in red) drawn through a single row in the floodmap. The mean energy resolution from this data was 12.7% FWHM, with mean coincidence timing resolution of 348ps FWHM.

The dynode signal will also be used to generate the readout trigger. A copy of the signal will be separately shaped so as to have symmetric rise and fall times and then sampled by a 100 Msps ADC. The event timing will be extracted from the sampled waveform with 312 ps granularity, corresponding to 5 bits of timing information for each 10 ns sample. Each of the individual ROCSTAR boards will send these 5-bit timestamps to a Master Coincidence Unit (MCU) in order to form coincidence triggers. When a coincidence is found by the MCU, it will send a trigger back to the relevant pair of ROCSTAR boards, which will stop the DRS4 sampling and read out the events. Event data will be written out independently by each readout board over Ethernet, with UDP packets from the many readout boards feeding through an Ethernet switch to a single DAQ computer.

III. ELECTRONICS REQUIREMENTS

The performance requirements that are dictated by the detector are: discrimination of 1.5x1.5-mm^2 cross-section crystals in the detector flood map and 250 ps single detector timing resolution (corresponding to 350 ps FWHM coincidence resolving time). In addition, the breast-imaging application dictates operation at a maximum of 200kcps singles rate per PMT, with 10 kcps trigger rate after energy gate and coincidence logic [1]. The goal for these electronics is to provide a system that will enable this level of performance without grossly over-specifying the system and thus increasing the cost unnecessarily. To this end, a number of Monte Carlo simulations were performed in order to determine the minimum set of electronics specifications that should enable this level of detector performance. These would then serve as guidelines for designing the final system.

A. Crystal Discrimination

To design the signal path for the anodes we first sought to determine what was the minimum shaping time and signal shape that could be used. Then, based on that shape, simulations were run to determine what ADC sampling and bit rates would be sufficient to accurately measure the position. We also determined specifications for the level of analog noise and sampling jitter that could be tolerated. Specifications were determined based on these simulations that would measure the crystal location to within 5% of the intrinsic accuracy. That is to say, if the error in measured crystal position has an intrinsic width of 1 mm FWHM due to physical constraints, then the electronics should not contribute more than 0.05 mm FWHM of additional (absolute) error to the measurement.

B. Event timing

The event timing will be measured digitally from 1 to 5 Gsps waveforms captured by the DRS4 chip. The measurement jitter that is achievable with the DRS4 has been extensively studied, notably in [4], with sample jitters of < 2 ps rms being achieved in the best case. Our needs are more modest – an electronics timing resolution of 60ps FWHM (25 ps rms) would be sufficient to minimally impact the measured 350ps FWHM timing resolution of our detector, while an electronics timing resolution of 45 ps FWHM (19 ps rms) would be sufficient to minimally impact the timing of a system with 200 ps FWHM coincidence timing. We ran a simulation to determine the minimum sampling rate that will not degrade our timing, given the parameters of our crystal and PMT. Calculations were also made to determine the amount of analog noise and reference clock jitter that could be allowed without going over our specifications.

C. Event Rate

The DRS4 must be stopped while it is reading out captured events so there is an unavoidable dead-time that is inherent to its use. The coincidence trigger rate that is expected from the breast scanner is 10 kcps but the system is designed to accommodate 100 kcps for more specialized applications. We ran a queueing-type simulation to determine the expected dead-time as a function of both count-rate and DRS4 readout window size.

IV. RESULTS AND DISCUSSION

A. Specification for Crystal Discrimination

The effect of shaping time on crystal discrimination was studied with a Monte-Carlo simulation. The simulation modeled simplified light sharing and assumed a 1.5x1.5 mm^2 crystal with light spread evenly across the face. We started by assuming perfect electronics (continuous integration, no noise or jitter) and reducing the amount of simulated light collection until the FWHM of the simulated crystal location degraded by 5%. This allowed us to set a limit on the time constant of the anode shaping as faster shaping results in less charge integration. The simulation showed that the integration fraction could be reduced to as low as 30% without causing more than 5% degradation in crystal location. The anode shaping circuit on ROCSTAR uses tail cancellation with a 20 ns decay time (for LYSO), corresponding to a ~50% reduction in integrated charge – a level which resulted in a 3% degradation in our simulation. The simulated pulse shaping is shown in fig. 4 (left).

The same simulation was then modified to study the errors induced in the measured charge of each anode sum by the effect of sampling. The signal shape from fig. 4 ('Final shape', left) was 'sampled' at sampling rates from 33 Msps to 125 Msps, with each event having a random phase with respect to the sampling. The sampled signals were integrated over a varying number of samples and the FWHM of the simulated crystal locations was calculated. The resolution of the measurement was sufficient over the full range, though it appears to degrade rapidly at the lower end (fig. 4, right). To maintain compatibility with the existing trigger board (MCU) we chose to use 100 Msps ADCs for ROCSTAR, even though the simulation shows that we could have chosen a lower sampling rate.

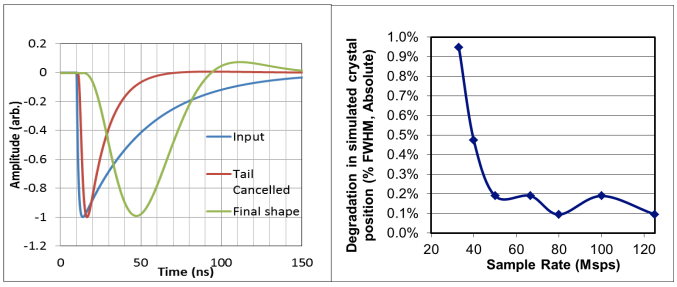

Fig. 4. Left: simulated pulse shapes for anode shaping. Right: results of simulation showing degradation in crystal discrimination due to sampling effects.

Finally, the real-world effects of analog noise, ADC bit rate (quantization noise), and sampling jitter were added into the simulation. The simulation assumed 50% charge integration and 100 Msps sampling, with the signals being integrated over 10 samples. The electronics parameters were again varied to find which values would result in a 5% FWHM error in crystal location. This simulation found values of 7 bits, 10 mV rms electronics noise, and 5 ns rms sampling jitter.

B. Specifications for Timing

A simulation was run to determine the minimum acceptable sampling rate for the dynode signal waveform. A pulse model was constructed that modeled the crystal's and PMT's contributions to the pulse shape (crystal light output and decay, PMT quantum efficiency, transit-time spread, and risetime). The simulated pulses were sampled at 2-5Gsps. When the relevant parameters from the H8500 (0.8 ns risetime, 0.4 ns TTS) and an ideal LYSO crystal (42 ns decay, no optical photon path length effects) were input to the model, the simulation generated the data plotted in fig 5. These data indicate that a sampling rate of 3 Gsps or greater is required to maintain the timing performance of the detector. This is not surprising as the fast 0.8 ns risetime of the H8500 PMT necessitates fast sampling to capture sufficient samples on the leading edge.

The DRS4 has been shown to be capable of achieving measurement jitter as low as ~5 ps FWHM when each channel is individually calibrated. More simple calibration methods result in measurement jitter in the 40ps FWHM range [2]. Assuming a risetime of 2.5 ns and a 500 mV average pulse amplitude, each millivolt (rms) of noise will contribute ~12 ps FWHM error to the timing measurement. ROCSTAR makes the timing measurement by comparing the leading edge of the timing signal with the nearest edge of the reference clock that is distributed from the MCU. Because of this, the jitter of the

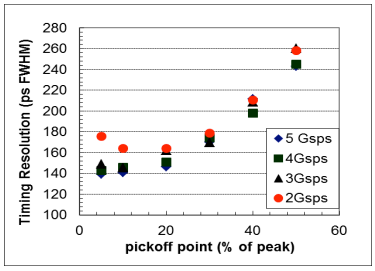

Fig. 5. Results of simulation to determine minimum sampling rate for good timing resolution. Simulation assumed the use of the H8500 PMT (0.8 ns risetime, 0.4 ns TTS) with an ideal LYSO crystal (42 ns decay, no optical photon path length effects).

reference clock will also add directly to the measurement uncertainty. The electronics parameters that are required to accurately measure 350 ps FWHM coincidence timing and 200 ps FWHM coincidence timing are detailed in table 1. It is particularly worth noting that the 'basic' DRS4 calibration (40 ps FWHM) is sufficient for 60 ps FWHM electronics timing resolution but a more accurate calibration is required in order to reach 45 ps FWHM electronics timing resolution. The board will need to be designed with the option of applying calibration waveforms individually to each DRS4 channel in order to meet the more stringent timing specification.

Target Electronics Timing Resolution	**60 ps FWHM**	**45 ps FWHM**
DRS4 Calibration	40 ps FWHM	30 ps FWHM
Ref. Clock Jitter	30 ps FWHM	25 ps FWHM
Analog Noise	3 mV rms	2 mV rms

Table 1: Electronics parameters required to achieve given timing performance. 60 ps FWHM electronics timing resolution is sufficient to accurately measure 350 ps FWHM CRT while 45 ps FWHM electronics timing resolution is required to accurately measure 200 ps FWHM CRT.

C. Specifications for Event Rate

A queuing-type simulation was also run to study pulse pileup and readout deadtime. The simulation assumed two opposing detectors with 6 PMTs each. The per-PMT singles rate was fixed at 200 kcps and the coincidence rate was varied between 5 and 100 kcps. Fig. 6 shows the results of this simulation. There was no appreciable dead-time at the lower coincidence rates but it was clear from this simulation that two DRS4s in a ping-pong configuration were absolutely required to reduce dead time at the higher rates. At higher count rates, a shorter DRS4 readout window should be used to avoid excessive dead-time.

The simulation also modeled pulse pile-up and random triggers. At a singles rate of 200 kcps per PMT the percentage of events with a time separation of less than 150 ns was 10%. This indicates a need for at least modest tail cancellation on the dynode signal to mitigate pulse pile-up. If we also assume a 10 kcps coincidence rate then the percentage of random triggers was 20% with the coarse trigger (6 ns window) and 8% with the final timing cut (2 ns window).

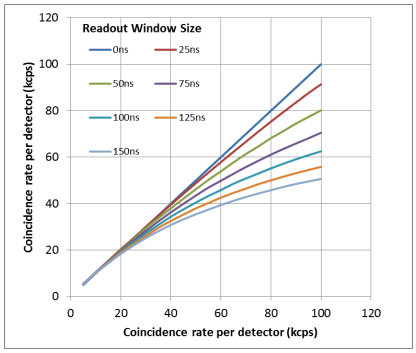

Fig. 6. Results of event rate simulation: Plot of the measured versus true coincidence rate per detector module. The calculations assume 2 DRS4s operating in a 'ping-pong' configuration.

D. Prototype Results

Two prototypes have been produced to date in order to prove that the analog portions of the design will meet the specs laid out in the previous sections. As mentioned previously, an active row-column summing unit for the H8500 was produced in 2012 that was used in performance studies, which were reported in [1]. However, the row-column summing board did not include any shaping so a second prototype was produced to verify the shaping for both the anode (position) and dynode (timing, energy) portions of the board. The anode signal chain will include a VGA in order to correct for variations in response across the face of the PMT before row-column summing. VGAs are known to be noisy so it was important to verify the noise performance of this portion. The resulting prototype showed an additive noise level of 0.45 mV rms for one full row/column sum. This is well below the specification of 10 mV rms established in the previous section. The shaping circuit was also verified, with the average measured pulse shape shown in fig. 7. The shape of the pulse is important for accurate charge integration, requiring a symmetric rise and fall, with only a minor undershoot.

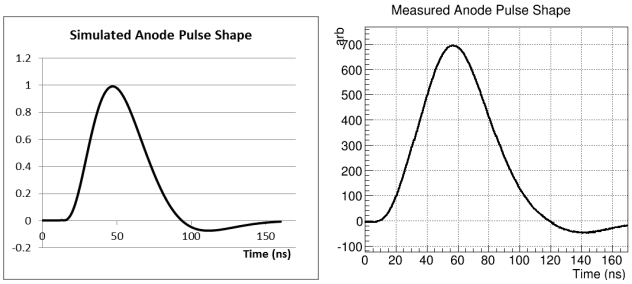

Fig. 7. Left: simulated anode pulse shapes. Right, measured anode pulse shape from shaping prototype board.

The timing performance of the dynode shaping chain was also studied using the shaping prototype board. The dynode shaping uses slight tail cancellation to reduce pulse pile-up. However, the tail cancellation reduces the integrated charge as well as accentuating higher frequency noise in the signal so it should be applied carefully. Table 2 shows the results obtained using the shaper prototype with a 4 x 4 x 20 mm^3 LYSO crystal. The most aggressive shaping had a clear negative affect on the timing performance but more moderate tail cancellation (20 ns time constant) did not greatly degrade the timing.

Effective pulse decay time (ns)	Coincidence Resolving Time (ps FWHM)
40 (no shaping)	240
20	250
10	270

Table 2: Prototype timing results with shaping. Note these tests were done with a 4 x 4 mm^2 crystal so the results are not directly comparable to previous tests done with the 1.5 x 1.5 mm^2 crystals which showed ~350 ps FWHM resolution.

V. Summary

Readout electronics are being developed to instrument a high resolution, time-of-flight PET scanner, targeted for breast imaging. The electronics and system design is a modular one, allowing the electronics to be used in many different system geometries. The electronics has been optimized for the H8500 PMT but it could be used to instrument a wide range of other rectangular photosensor arrays. The design of the electronics was presented, along with the results of simulations which were used to determine a set of electronics specifications. The simulations provided valuable guidance in setting out the design of the board. In particular the simulations indicated the need for channel-by-channel DRS4 calibration (to reduce sample jitter) as well as having two DRS4 chips in parallel (to reduce dead-time). The simulations also guided our choice of pulse shaping for the anode/positioning portion of the circuit. Prototype results show that the design falls well within the specifications that we had established.

The ROCSTAR board is still under development, with both circuit design and FPGA logic design complete. PCB layout is underway as of this writing.

References

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