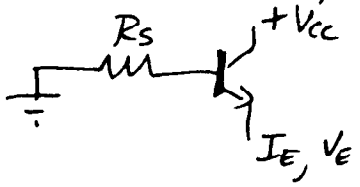
CHAPTER 2

Transistors (bipolar)

Physics 123
PROBLEM SET #4 - SOLUTIONS

2.1 Assume the transistor is in the active region (i.e., don't worry about bias), and apply a wiggle ΔV_E at the emitter:



Make a change ΔV_E; then

$$\Delta V_B = \Delta V_E$$
$$\Delta I_B = \Delta V_B / R_S = \Delta V_E / R_S$$
but $\Delta I_C = h_{fe}\,\Delta I_B$
and $I_E = I_B + I_C$

$$\text{so, } \Delta I_E = \Delta I_B + \Delta I_C = \frac{\Delta V_B}{R_S}(1+h_{fe}) = \frac{\Delta V_E}{R_S}(1+h_{fe})$$

giving an output resistance (small signal - incremental) of

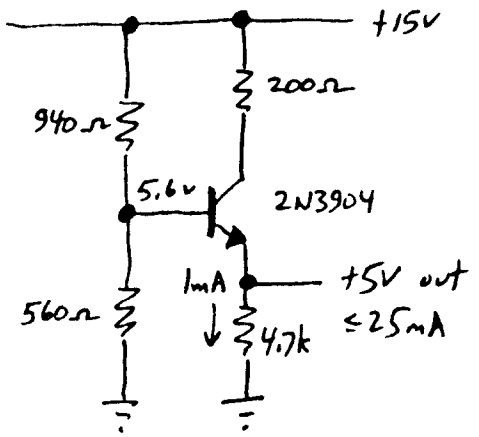
$$r_e = \frac{\Delta V_E}{\Delta I_E} = \frac{R_S}{1+h_{fe}}$$

To generalize to impedances, replace R_S by $\underset{\sim}{Z_S}$
I_E by $\underset{\sim}{I_E}$
V_E by $\underset{\sim}{V_E}$
V_B by $\underset{\sim}{V_B}$
I_B by $\underset{\sim}{I_B}$

2.2 ① choose V_B : 5.6 volts

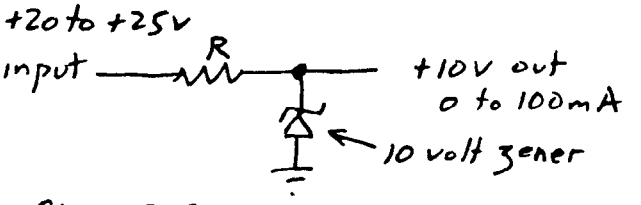
② want $\Delta I_E = 25\,mA$ to produce a ΔV_B less than 0.2 V; since this $\Rightarrow \Delta I_B$ of $\approx 0.25\,mA$, the base divider must look like $\leq 800\,\Omega$

③ Include emitter resistor for small emitter current in absence of external load



④ $R_c = 200\,\Omega$ for current limiting

2.3 Worst-case (minimum zener current) is $V_{in} = 20V$, $I_{OUT} = 100mA$.

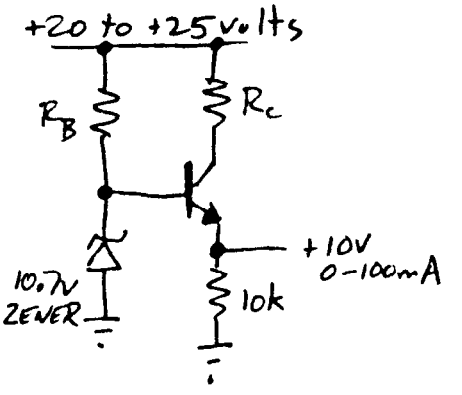


Thus, $R = \frac{V_R}{I} = \frac{20-10}{0.110} = \underline{91\Omega}, 2.5W$

Power: Worst-case is $V_{in} = 25V$, $I_{OUT} = 0mA$.

Then $P_{ZENER} = I_Z V_Z = \frac{25-10}{R} \times 10 = \underline{1.65 \text{ Watts}}$

2.4



Assume $h_{FE} \approx 100$. Then, as before,

R_B determined by

$$\frac{20-10.7}{R_B} = \frac{100mA}{h_{FE}} + 10mA = 11mA$$

$\Rightarrow R_B = \underline{850\Omega}, \frac{1}{4}W$

R_c limits current; $R_c = \underline{68\Omega}$, 1W is good

(transistor still in active region - $V_{CE} = 3.2V$ - at max load)

Power: Worst-case for transistor is $V_{in} = 25V$, $I_o = 100mA$

$P_T = 0.8W$

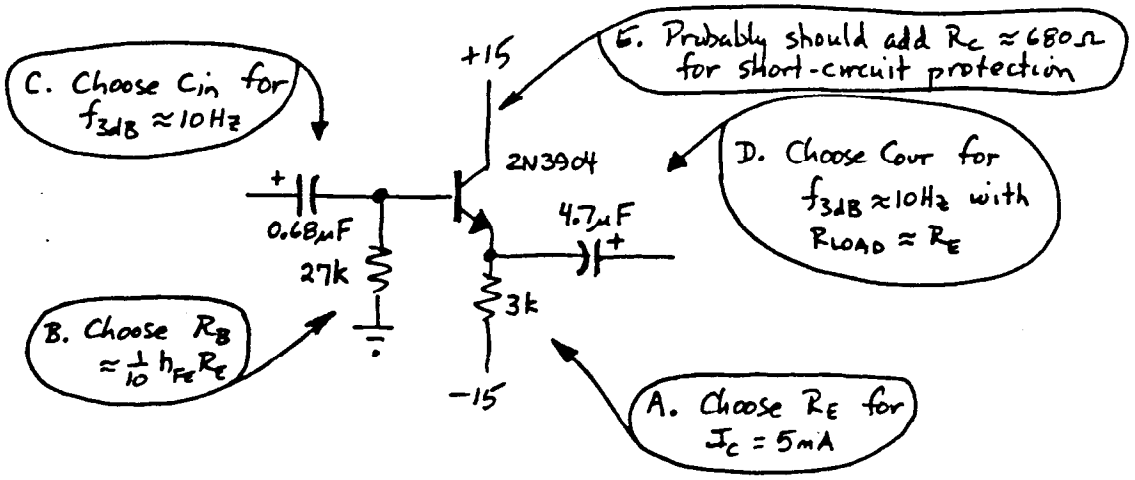
Worst-case for zener is $V_{in} = 25V$, $I_o = 0mA$

$P_z = 0.18W$

% change in I_z, $11mA \rightarrow 10mA$: 10%

Previous circuit: $\begin{cases} \%\,\Delta I_z = 1000\% \quad (110mA \rightarrow 10mA) \\ P_T = 0 \\ P_z = 1.65W \end{cases}$

2.5

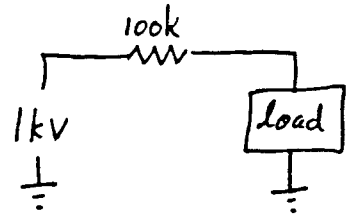


2.6

For ±1% variation with ±5 volt load variations, need 500v in series with a resistor. "Constant to 1%" might mean ±½%, in which case you need 1000v + resistor.

2.7

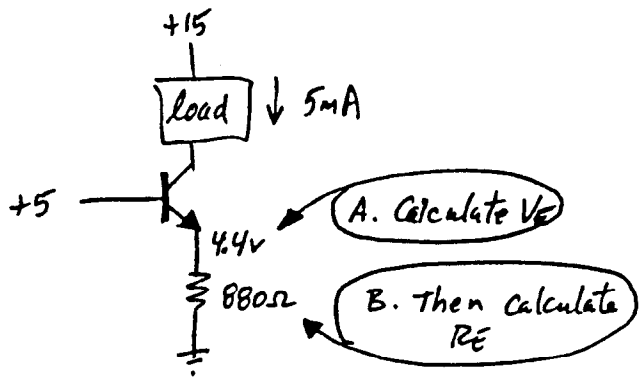
Take the ±½% specification:



$P_R = 10W$

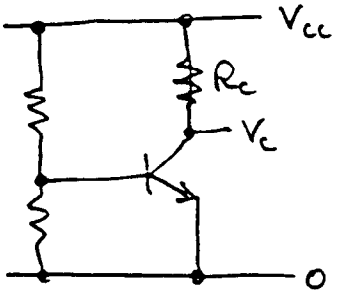
P_{load} (max.) = 10v × .01A = 0.1W

2.8



Output compliance ≈ 10.4 volts ($V_{CE(SAT)} \approx 0.2V$)

2.9



V_c at the bias point is $V_{cc}/2$
For V_c to drop to zero the voltage across R_c must double, $\Rightarrow$ I_c must double

$I_c \propto e^{V_{BE}/V_T}$

$\Rightarrow$ V_{BE} must change by $V_T \log 2$

Instead, V_{BE} is fixed, and the temperature changes the effective V_{BE} (at the rate of 2.1 mV/degC).

$$\Rightarrow \quad \Delta T = \frac{V_T \log 2}{2.1\,mV} = \frac{25.3 \times 0.69}{2.1} = 8.3 \text{ deg C.}$$

2.10 (same circuit as 2.9)

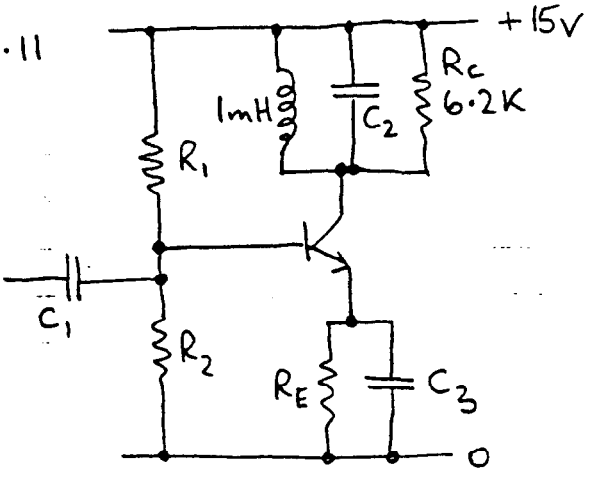
$$\text{Gain} = \frac{R_c}{r_e} \qquad r_e = \text{intrinsic emitter resistance} \simeq \frac{0.025}{I_c \text{ (amps)}}$$

$$G = \frac{R_c}{0.025/I_c} = \frac{R_c I_c}{0.025}$$

Collector biased to $V_{cc}/2$ has $V_{cc} - V_c = R_c I_c = V_{cc}/2$

$$\Rightarrow \quad G = \frac{V_{cc}}{2 \times 0.025} = 20\, V_{cc}$$

2.11



i) Tuned circuit

$LC_2 = \frac{1}{\omega^2}$ $\quad C_2 = \frac{1}{\omega^2 L} = \frac{1}{40 \times 10^{10} \times 10^{-3}}$

$= 2500\ pF$

Tuned amplifier : gain at DC = 0

gain at 100kHz (when parallel LC circuit has infinite impedance) is : $G(100kH_z) = \frac{R_C}{r_e} \simeq 250$

ii) Bias the emitter to $+2{\cdot}2v \Rightarrow R_E = \frac{2{\cdot}2v}{1{\cdot}0mA} = 2{\cdot}2K$

iii) The base is then at 2.8v ; 0.1 mA divider current will suffice (ten times the base current)

$\Rightarrow R_2 = 27K$, $R_1 = 120K$

iv) C_3 should be chosen so that $|X_{C_3}| \ll r_e \simeq 25\Omega$

$\Rightarrow C_3 \gg \frac{1}{\omega r_e} = \frac{1}{8 \times 10^5 \times 25} = \cdot 6 \times 10^{-7}$. Choose $1{\cdot}0\mu$

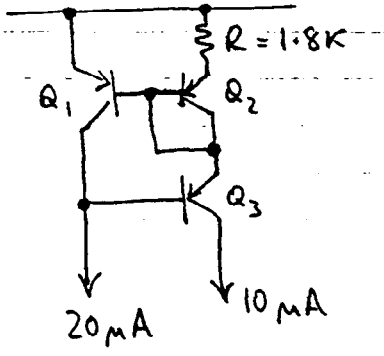
v) $Z_{in} = (\beta+1) r_e \,||\, (R_1 \| R_2) = 2{\cdot}5k \,||\, 20k = 2{\cdot}5k$ (100kH

C_1 should be chosen so that $|X_{C_1}| \ll Z_{in}$

$\Rightarrow C_1 \gg \frac{1}{\omega Z_{in}} = \frac{1}{6 \times 10^5 \times 2500} = \cdot 6 \times 10^{-9}$ Choose $0{\cdot}01\mu F$

NB Since the amplifier is only required to work at high frequencies, quiescent biasing of the collector to $V_{cc}/2$ is not required. Indeed the collector here is at V_{cc} when no signal is applied.

2.12



10 μA flows through Q_2 and Q_3 and hence through R.

This introduces a ΔV_{BE} of :

10mA × 1·8K = 18mV between Q_1 and Q_2

From figure 2.51, the ratio of collector currents is 0·5 at 25°C

This agrees with the 10mA / 20mA ratio claimed.

2.13 $G_{diff} = \frac{R_C}{2(R_E + r_e)}$ is maximum when $R_E = 0$.

$r_e = \frac{.025}{I_C \text{ (amps)}} \Rightarrow G_{diff} = \frac{R_C I_C}{2 \times .025} = 20 R_C I_C = 20 V_{R_C}$

where V_{R_C} is the voltage across the collector load resistor at the quiescent bias point.

Similarly $CMRR = \frac{R_1}{R_E + r_e}$ is max for $R_E = 0$

$CMRR = \frac{R_1}{r_e} = \frac{R_1 I_C}{.025} = 40 R_1 I_C = 20 V_{R_1}$

where V_{R_1} is the voltage across R_1 (NB $2I_C$ flows thro' R_1

2.14 Miller effect is introduced by capacitative coupling between C and B. This will only limit the high frequency performance of an amplifier stage when there are signals at both the collector and base. It is therefore completely absent in both grounded collector and grounded base configurations.

Fig 2.72 A Q_1 : gnd C.
Q_2 : gnd B.

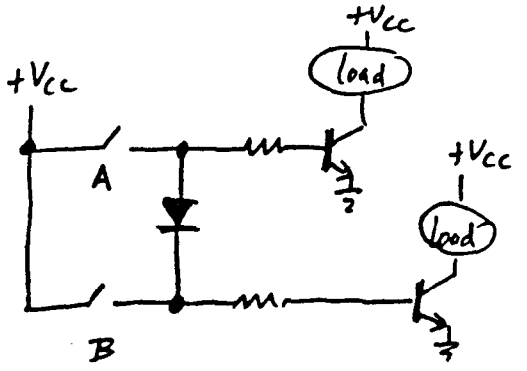
Fig 2.72 B Q_1 : gnd C (C is tied to 2.4V by the cascode Q_2)
Q_2 : gnd B.

CH2 BAD CIRCUITS

A. No bias ; wrong transistor polarity ; wrong polarity.
B. Zener has no bias current
C. Transistors interchanged : emitters to output.
D. Wrong polarity.
E. +5v will burn out both bases :- limiting R needed.
F. Bad bias on Q_2.
G. Lower transistor is a clamp, not current source.
H. Q_2 has no bias :- needs R from B_2 to $-V_{EE}$.
I. Thermally unstable. (works well for differential amp with current mirror)

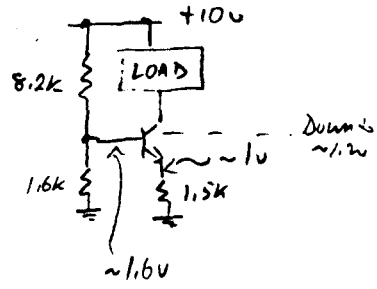
CH 2 Additional Exercises

AE 2-1



note: diode must be on "high" side of resistors — why?

AE 2



c.) What is I_{LOAD}?

$= V_E/R_E \approx \frac{1V}{1.5k} = 0.67mA = I_E \approx I_C$

Compliance: from about 1.2V ($V_E + V_{SAT}$) to +10V

b) Variation with β:

β varies from 50 to 100: how much variation in I_C

1 – Affects I_C directly, since $I_E = I_C + I_B$

2 – Affects I_C indirectly by altering V_B and thus V_E and thus I_E.

→ 1 – Direct Effect on I_C:

$I_E = I_B + \frac{I_C}{\beta}$: If β varies from 50 to 100,

I_E varies from 102% of I_C to 101% of I_C;

ie. if I_E is fixed, I_C varies by 1% (with β)

2 – Indirect effect on I_C:

Loading of base divider varies with β.

Thus stays ~ ±1.8% with β

$8.2k \| 1.6k \approx \frac{8k}{6} = 1.3k$

$V_{TH_{DIV}} \leftarrow \frac{1.6}{9.8} \cdot 10V = 1.6V$

ΔI_B is $\frac{I_C}{100} - \frac{I_C}{50} = \frac{I_C}{100}$

$\approx \frac{I_E}{100} = \frac{0.67mA}{100} = 6.7\mu A$

$\Delta V_B = \Delta I_B \cdot R_{TH_{DIVIDER}} = 6.7\mu A \cdot 1.3k = 8mV$

If this is passed to V_E, to alter I_E,

variation is $\frac{8mV}{1V} = \frac{8}{100} = 0.8\%$ (with β)

c.) Early Effect

$\Delta V_{BE} = -10^{-4} \Delta V_{CE}$

ΔV_{CE} over compliance range is 9V $\Rightarrow$ ΔV_{BE} if I_C fixed would be −0.9 mV

But this changes V_E (since V_B is fixed and I_E is not)

$\Rightarrow$ 0.09% change, or about 0.1%

d.) Temp Effect

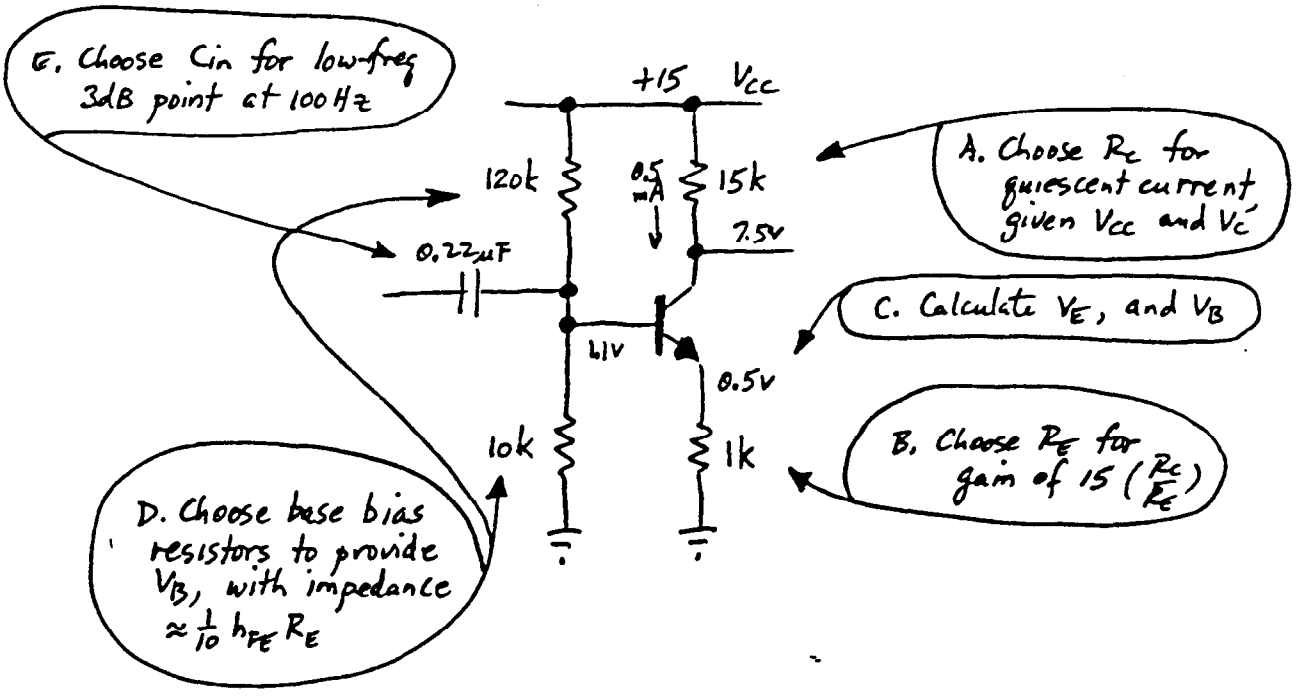
1 – Assuming h_{FE} constant: as for Early, first assume I_C fixed: $\Rightarrow \Delta V_{BE} = -2.1$

$\Rightarrow \Delta I_E = \Delta V_E / R_E = +\frac{2.1mV/°C}{1.5k} \approx +1.5\mu A/°C$

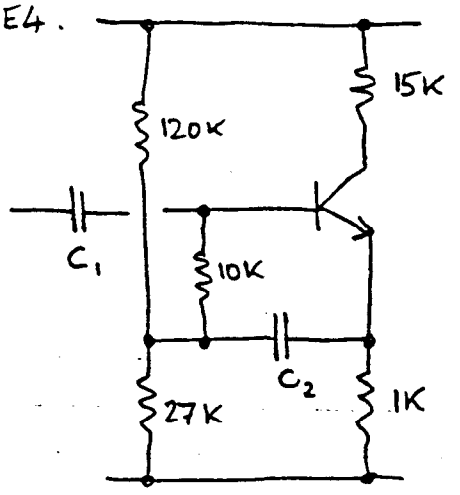
$\approx +0.2\%/°C$

2 – Assuming h_{FE} drops at 0.4%/°C:

@ Two effects (part b), then double this to 1%. But that's 1% of $\Delta h_{FE} = 61 \Rightarrow +0.02\%$ ×10



AE4.

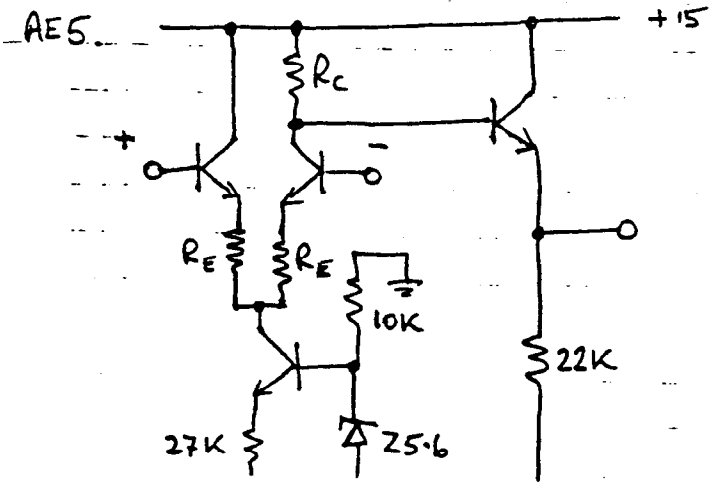


C_2 should be large enough that the bootstrap works down to the amplifier's 3dB point.

$C_2 > 0.68\,\mu F$ (same calc. as above).

Z_{in} is now at least 10x larger so $C_1 = .068\,\mu F$ is fine.

AE5.



Differential Gain, $G_{diff} = \dfrac{R_c}{2(R_E + r_e)} = 50$

Want ~7V across R_c to allow a large swing (inputs near ground)

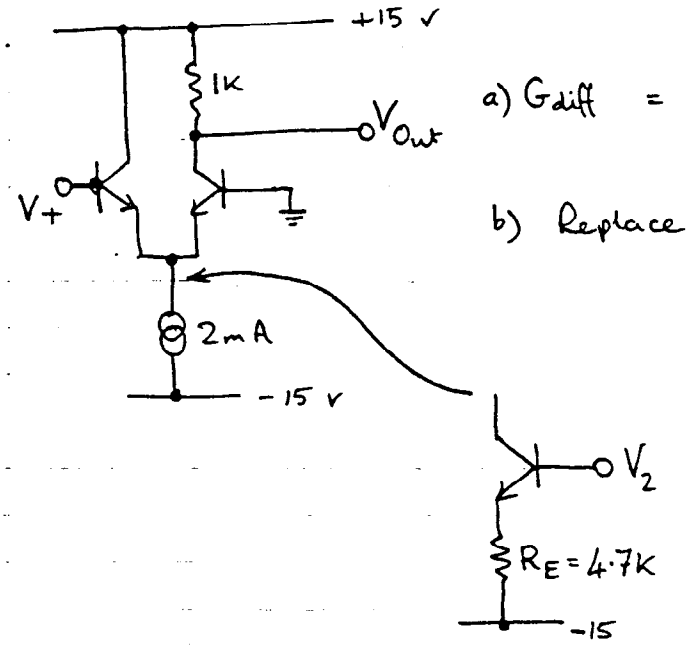
$\Rightarrow R_c = 7V / .1mA = 68\,K\Omega$

$\Rightarrow R_E + r_e = R_c/100 = 680\,\Omega$

$r_e = 25/0.1mA = 250\,\Omega$

$\Rightarrow R_E = 470\,\Omega$

AE6.



a) $G_{diff} = \frac{R_c}{2r_e} = \frac{R_c I_c(mA)}{50} = 20$

b) Replace current source with:

Current through long-tail pair is now:

$2I_c = \frac{(V_2 - 0.6 + 15)}{R_E}$

With $R_E = 4.7K$:

$I_c = \frac{(V_2 + 14.4)}{10}$ mA.

The gain is now $G = \frac{R_c I_c}{50} = \frac{1000}{50}\frac{(V_2 + 14.4)}{10} = \frac{V_{out}}{V_+}$

$\Rightarrow V_{out} = 2 V_+ (V_2 + 14.4)$

The multiplier is subject to the constraints:

i) V_+ near ground

ii) $-14 < V_2 < \min(V_+, 0)$

AE7 a) $I_C = 1mA \quad r_e = 25\,\Omega$

$Z_{in} = 100 \times 25\,\Omega \parallel 1K \parallel < 100\,\Omega = < 100\,\Omega$ (setting of the variable resistor)

b) $G = \frac{10K}{25\,\Omega} = 400$

c) Same as 2.9 : 8.3 deg C.

AE8. The base current of Q_2 is equal to that of Q_1 since the have the same I_c and same β (matched).

This current is mirrored by Q_3 and Q_4 and used to drive the base of Q_1.

So with no input applied, Q_1 is biased into conduction (this is <u>not</u> true for a normal diff. input stage), and the <u>additional</u> (+ve or -ve) current supplied when the input is connected is what is amplified.

I.E. the input draws no <u>bias</u> current from the signal source.