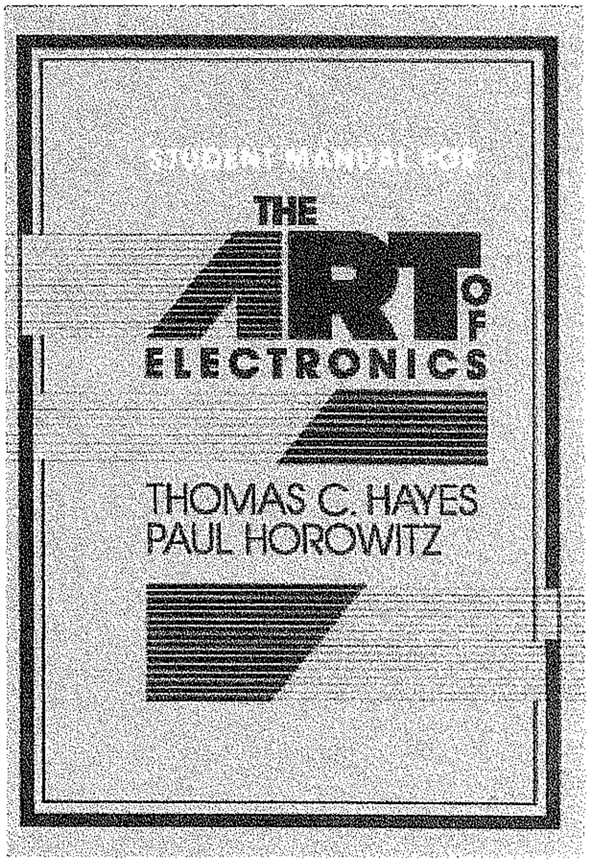

STUDENT MANUAL FOR

THE ART OF ELECTRONICS

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12L.2 Analog Switches

The CMOS analog switch is likely to suggest solutions to problems that would be difficult without it. This lab aims to introduce you to this useful device. Schematically, it is extremely simple: it simply passes a signal or does not:

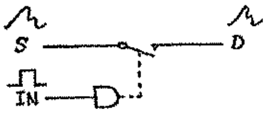

Figure 5: Analog switch: ***generic***

The switch we are using has especially nice properties: it is switched by a standard logic signal, 0 to +5 (High, +5 = ON). But it can handle an analog signal anywhere in the range between its supplies, which we will put at 15 volts. It also happens to be a *double-throw* type, nicely suited to selecting between two sources or destinations.

Here is the switch, and its pinout:

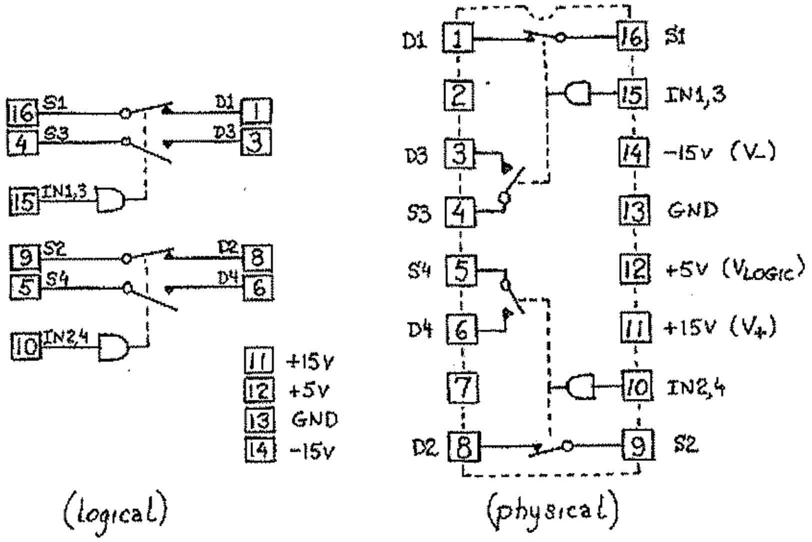

Figure 6: DG403(Maxim) analog switch: block diagram and Pinout

As signal source use an external function generator; as source of the "digital" signal that turns the switch on or off use one of the slide switches on the breadboard. The easiest to use is the 8-position switch: put one of its slides in the ON position; now that point will be high or low, following the position of the slide switch just to the right of the "DIP" ("dual in-line package") switch.

Caution: each package contains two switches. Tie the unused "IN" terminal to ground or to +5 (this makes sure the logic input to the switch does not hang up halfway, a condition that can cause excessive heating and damage.)

And a *reminder*: this IC uses *three power supplies*: connect all of them!

12L.2.1 R_{on}

Time: 10 min.

Ideally, the switch should be a short when it is ON. In fact, it shows a small resistance, called R_{on}. Measure R_{on}, using the setup shown below:

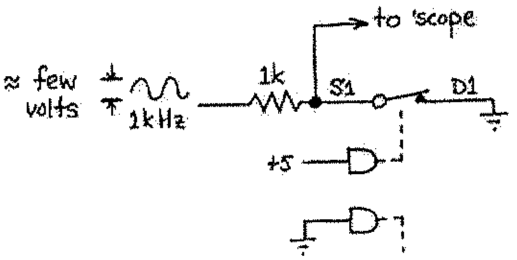

Figure 7: R_{on} measurement

Use a 1 kHz sine of several volts' amplitude. Confirm that the switch does turn On and Off, and measure R_{on}.

Time: 10 min.

12L.2.2 Feedthrough

The circuit below makes the switch look better: its R_{on} is negligible relative to the 100k resistor. Confirm this.

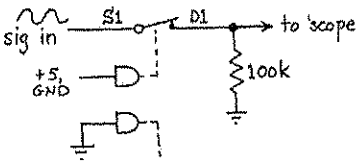

Figure 8: More typical application circuit (R_{on} made negligible)

When the switch is OFF, does the signal pass through the switch? Try a high-frequency sine (¿100 kHz). Try a square wave. If any signal passes through the OFF switch, why does it pass?

Note: as you do this calculation, don't forget that you are looking at the output with a scope probe whose capacitance (to ground) may be more important than its large R_{in}: you're really watching a *capacitive divider* at work. So long as you don't forget this probe capacitance, you should have no trouble calculating the switch's C_{DS}.

Time: 10 min.

12L.2.3 Chopper Circuit

Here is a cheap way to turn a one-channel scope into two channel (and on up to more channels, if you like). (Query: what are the limitations on this trick?)

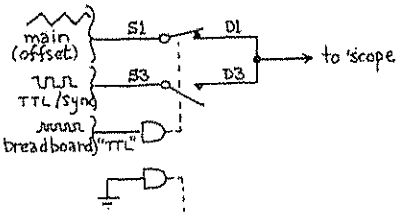

Figure 9: Chopper circuit: displays two signals on one scope channel

For a stable display, trigger on one of the input signals, not on the chopper's output, where the transients will confuse your scope.

Time: 20 min.

12L.2.4 Sample & Hold

This application is much more important. It is used to *sample* a changing waveform, *holding* the sampled value while some process occurs (typically, a conversion from analog into digital form).

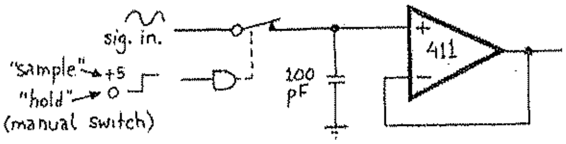

Figure 10: Sample & hold

Try the circuit. Can you infer from the droop of the signal when the switch is in *hold* position, what leakage paths dominate? (This will be hard, even after some minutes of squinting at the scope screen; don't give your afternoon to this task!)

Query: how does one choose C value? What good effects, and what bad, would arise from choice of a cap that was a) very large; b) very small?

Can you spot the effect of *charge injection* immediately after a transition on the control input? Compare the specified injection effect and the voltage effect you would predict, given the specification (≤ 60 pC, typical, for the DG403) and the value of your storage capacitor.

Optional: a dynamic view of charge injection

If you inject charge periodically, by turning the switch on and off with a square wave, you can see the voltage error caused by charge injection in vivid form[3] The *held* voltages ride above the input, by a considerable margin; you will notice the margin varies with the waveform voltage. Why?

Good sample & hold circuits evidently must do better, and they do. See, e.g., the AD582 with charge injection of ≤ 2 pC; and see Text §3.12, p. 149.

12L.2.5 Negative Supply from Positive ("Flying Capacitor")

Time: 10 min.

You know that a switching regulator can generate a negative output from a positive input, with the help of an inductor. For low-current applications the circuit below, which requires no inductors, sometimes is preferable. The trick is to do a little levitation by shoving "ground" about in a sly way. A similar use of "flying capacitors" can generate a voltage larger than the input voltage.

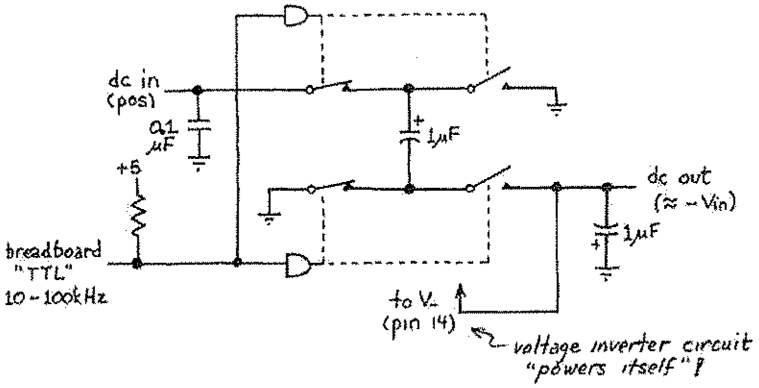

Figure 11: "Flying capacitor" voltage inverter

This circuit provides only a small output current, as you can confirm by loading it.

Such circuits often are put onto an integrated circuit that would otherwise require either a negative supply or a second positive supply, higher than the main supply [4].

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[3] Thanks to two undergraduates for showing us this technique: Wolf Baum and Tom Killian (1988).

[4] Semiconductor memories, for example, sometimes require such a supply. Once upon a time asked the user to supply +12V as well as +5V. The flying-capacitor trick ended this demand placed on the user; the chip solved the problem internally.

12L.2.6 Switched-capacitor Filter, homemade ~~and integrated~~

12L.2.6.1 Switched-capacitor Filter I: built up from parts

AoE §??

Time: 15 min.

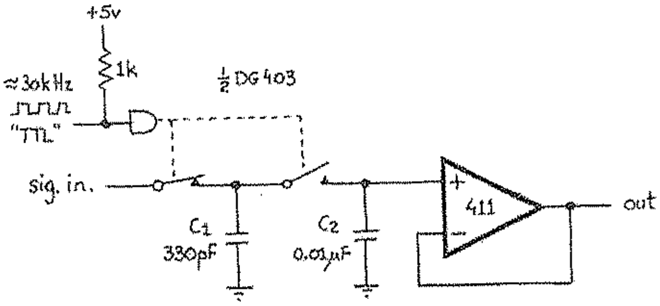

Figure 12: Switched-capacitor low-pass filter

This filter's f_{3dB} is regulated by the clock rate. This makes it a type convenient for control by computer. The Text sets out a general formula for f_{3dB} of this filter type (a "recursive filter," in the language of digital filtering). Given the values used here, this formula predicts

$$f_{3dB} = (0.03/2\pi) X f_{clock} \tag{12L.1}$$

Try the circuit, and compare its f_{3dB} with the predicted value. Does the filter behave generally like an RC filter: does it show the same phase shift at f_{3dB}? Does f_{3dB} vary as you would expect with clock frequency? Does the filter fail at the high end of the oscillator's range? Because this is a "sampling" filter, you can expect it to get radically confused when the input signal changes quickly relative to the rate at which the square wave transfers samples (the "sampling rate"). (This radical confusion is called "aliasing.") We'll look at the sampling-rate issue in depth when we reach analog-to-digital conversion, in Lab 18. For now, be warned that you should expect trouble when the frequency of a sinusoidal input approaches one-half the "sampling rate" applied to the analog switch control inputs.

Do you see feedthrough of the clock signal?