PHYSICS 364 2010-10-25

Field Effect Transistors

Like BJTs, FETs are 3-terminal devices in which a small signal controls a much larger signal.

base controls I_{CE} ; gate controls I_{DS}.

(quoting HH) In an NPN BJT, $B \to C$ is a reverse-biased junction, so no current normally flows $B \to C$. When you forward-bias $B \to E$ junction, electrons enter the base from the emitter, but 99% of these electrons flow to the collector. Hence I_C vs. V_{BE}.

In a FET, the electric field produced by gate potential attracts or repels charge carriers, which enhances or depletes the density of carriers (hence conductivity) in the channel.

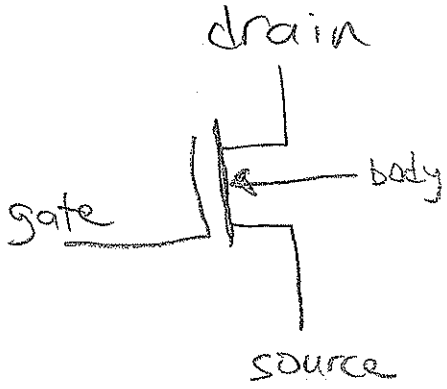
Motivation: NO DC current flows at the control electrode (called the "gate"). Result is huge input resistance $\sim 10^{14}\ \Omega$.

So then
- FET opamp has $I_{bias} \simeq 0$
- can store charge on capacitor for DRAM or Sample & Hold
- can make logic circuits with negligible quiescent current, hence negligible power except while switching between states

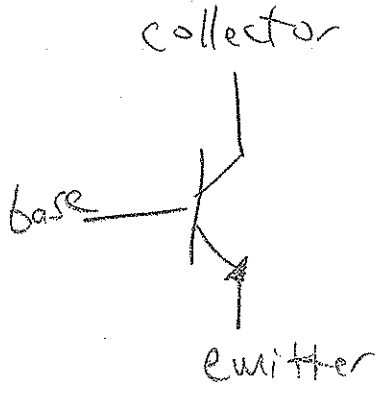
A confusing FET family tree

- n-channel vs. p-channel
- enhancement vs. depletion
- MOSFET vs. JFET
  (metal + insulator + semiconductor vs. back-biased pn junction at gate)

We'll focus on n-channel MOSFET for simplicity.



n MOS



NPN BJT

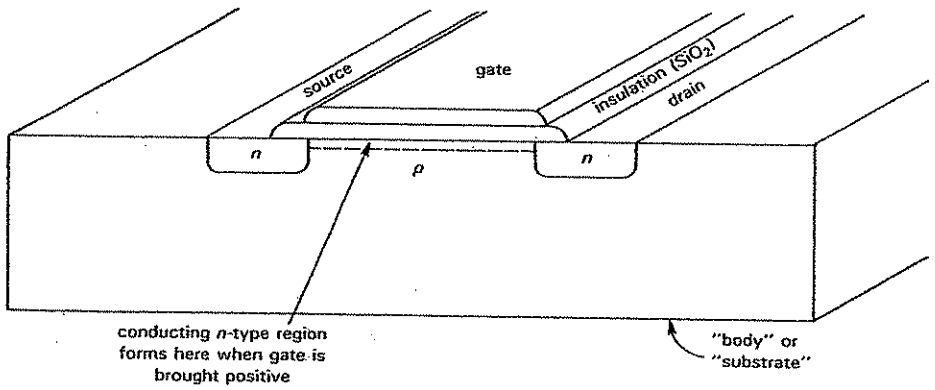


Figure 3.5. An *n*-channel MOSFET.

from HH p117

I_D vs. V_{DS} (V_{GS})

I_C vs. V_{CE} (V_{BE})

HH p. 115

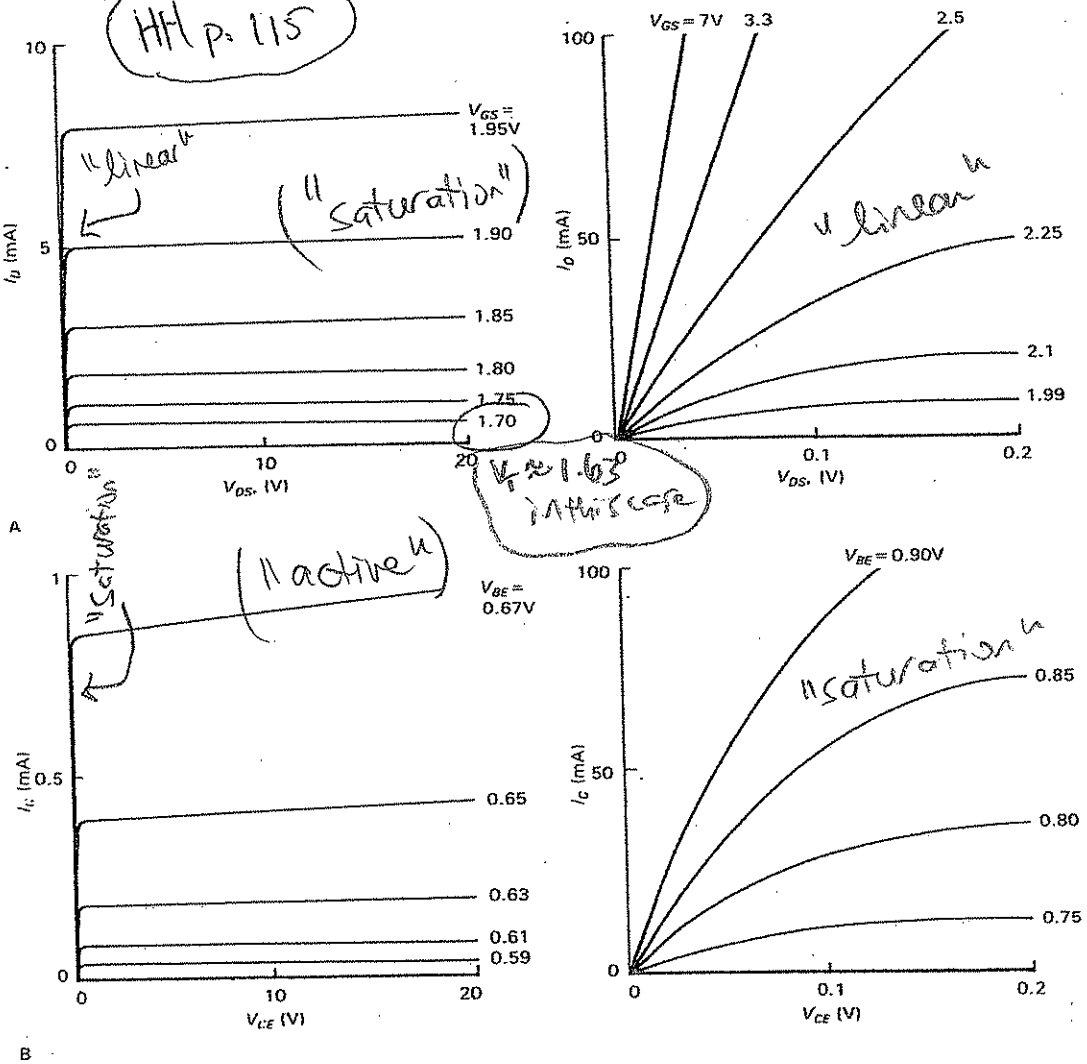
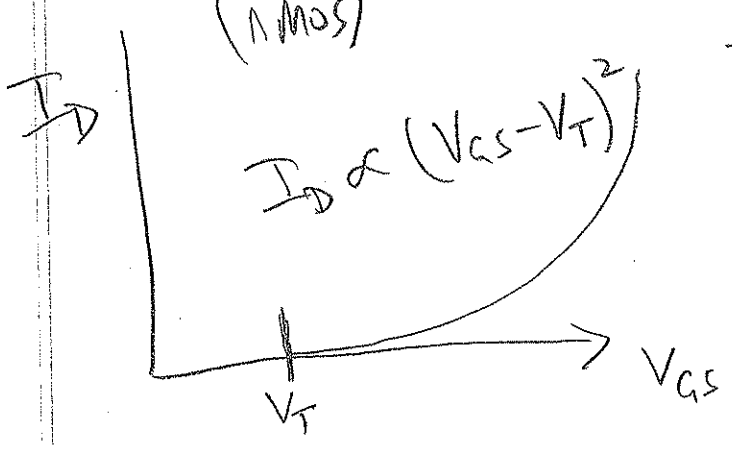


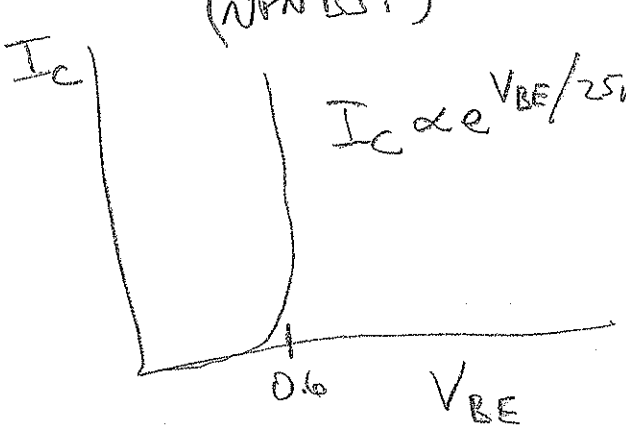
Figure 3.2. Measured MOSFET/transistor characteristic curves.
A. VN0106 *n*-channel MOSFET: I_D versus V_{DS} for various values of V_{GS}.
B. 2N3904 *npn* bipolar transistor: I_C versus V_{CE} for various values of V_{BE}.

In "saturation" (which means "active"!!) region, V_{GS} programs I_D, for sufficiently large V_{DS}.

(NMOS)



(NPN BJT)



Remember "r_e" $\equiv 1/\left(\frac{dI_C}{dV_{BE}}\right) = \frac{25mV}{I_C}$.

You can define "transconductance" $g_m \equiv \frac{1}{r_e}$

$= \frac{dI_C}{dV_{BE}} = \frac{I_C}{25mV} = \frac{I_C(mA)}{25\Omega} = .04 mho * I_C^{(mA)}$

Similarly, $g_m = \frac{dI_D}{dV_{GS}} = \frac{d}{dV_{GS}} k(V_{GS}-V_T)^2$

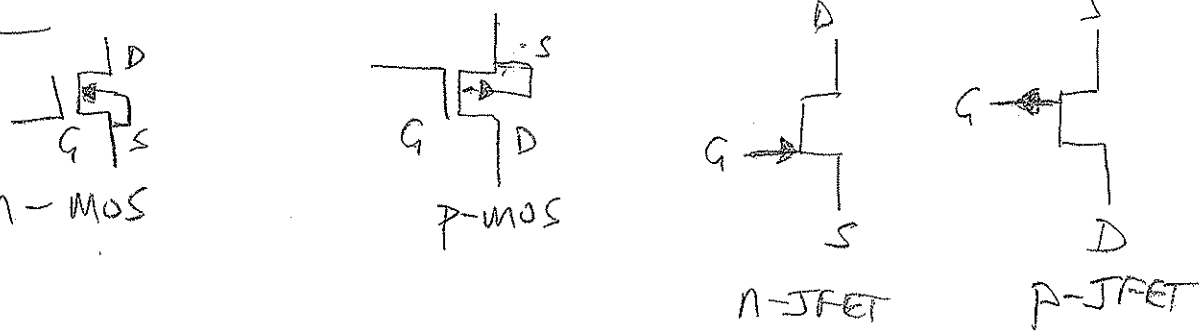
$= 2k \cdot (V_{GS}-V_T) = 2\sqrt{kI_D}$

(k in mA/V^2)

Incidentally, $kT \sim 1/2$, so $\not\exists$ thermal runaway

g_m for a FET tends to be much smaller than for a BJT $\Rightarrow$ "r_e" much higher.

This will come up in context of source follower, common-source amplifier, etc.



$I_D = k(V_{GS}-V_T)^2$

$g_m = 2k(V_{GS}-V_T)$

$= 2\sqrt{kI_D}$

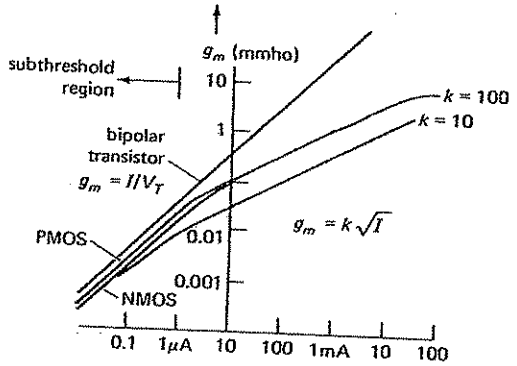


Figure 3.24. Comparison of g_m for bipolar transistors and FETs.

Figure 3.12 shows the situation schematically. In both regions the drain current depends on $V_{GS} - V_T$, the amount by which the applied gate-source voltage exceeds the threshold (or pinch-off) voltage. The linear region, in which drain current is approximately proportional to V_{DS}, extends up to a voltage $V_{DS(sat)}$, after which the drain current is approximately constant. The slope in the linear region, I_D/V_{DS}, is proportional to the gate bias, $V_{GS} - V_T$. Furthermore, the drain voltage at which the curves enter the "saturation region," $V_{DS(sat)}$, equals $V_{GS} - V_T$, making the saturation drain current, $I_{D(sat)}$, proportional to $(V_{GS} - V_T)^2$, the quadratic law we mentioned earlier. For reference, here are the universal FET drain-current formulas:

$$I_D = 2k[(V_{GS} - V_T)V_{DS} - V_{DS}^2/2] \quad \text{(linear region)}$$

$$I_D = k(V_{GS} - V_T)^2 \quad \text{(saturation region)}$$

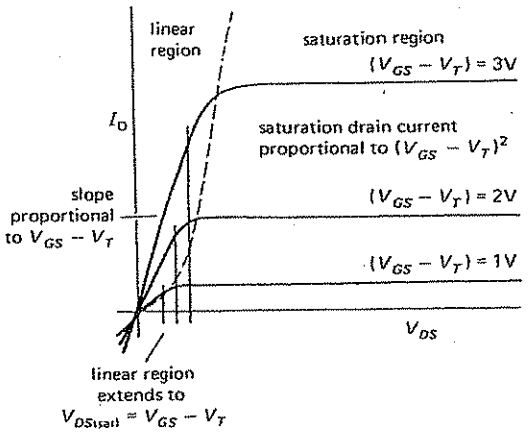


Figure 3.12

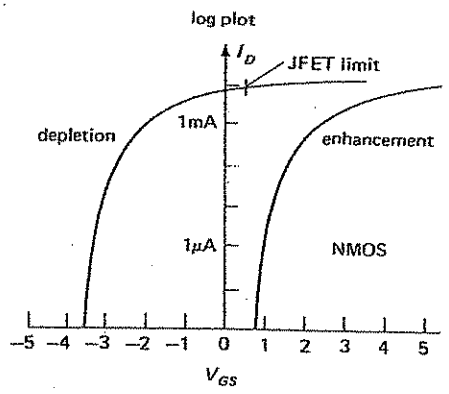


Figure 3.8

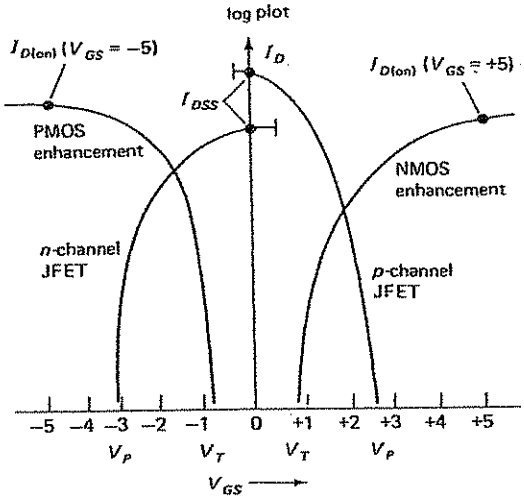


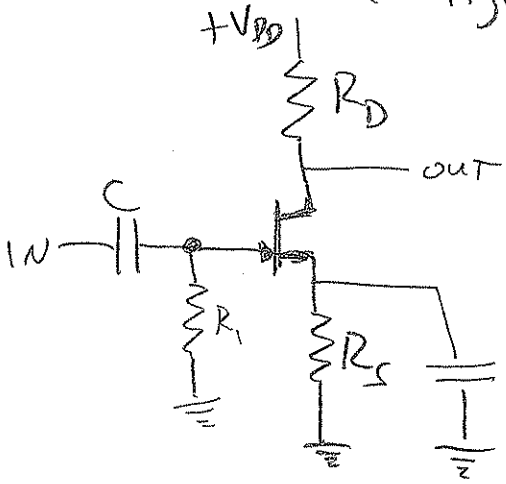
Figure 3.11

(depletion mode) JFET is "ON" at $V_{GS} = 0$; bring gate down to $V_{pinchoff}$ to shut OFF.

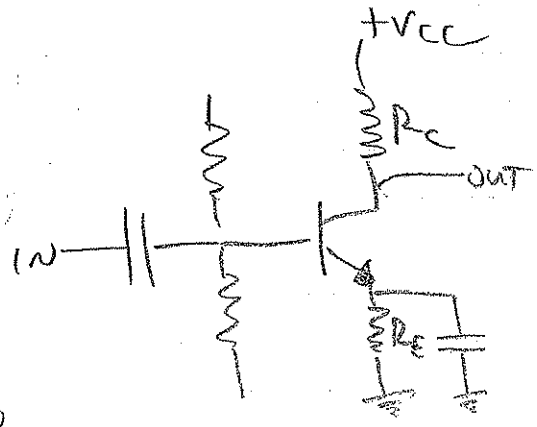
(enhancement mode) MOSFET is "OFF" at $V_{GS} = 0$; bring gate up to $V_{threshold}$ to begin to turn on.

$V_T \sim$ 0.8 – 2.4 volts in the MOSFETs we'll use today.

Consider a "common source amplifier" configured for maximal AC gain.

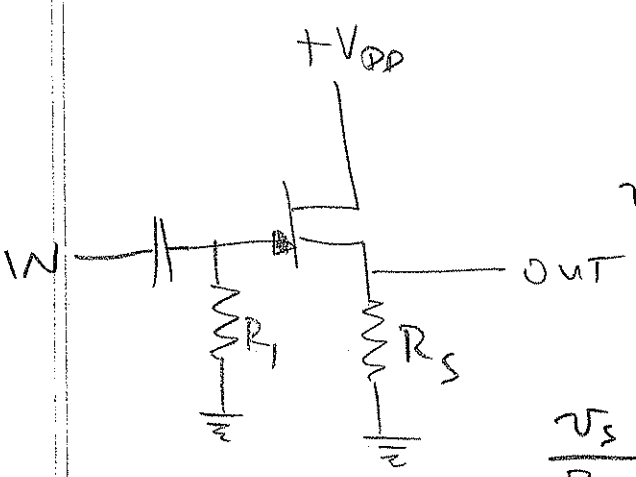


$$\frac{dV_{OUT}}{dV_{IN}} = -R_D \frac{dI_D}{dV_{gs}} = -g_m R_D$$



$$\frac{dV_{OUT}}{dV_{IN}} = -\frac{R_C}{r_e} = -g_m R_C$$

"source follower"



$$V_{OUT} = R_S I_D$$

$$v_s = v_{OUT} = R_S i_D \quad \text{(differential)}$$

$$i_D = g_m v_{gs} = g_m v_g - g_m v_s$$

$$\frac{v_s}{R_S} = g_m v_g - g_m v_s$$

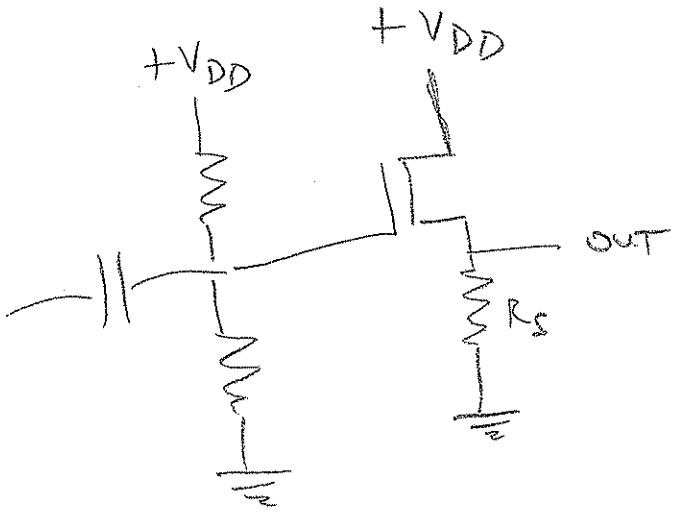
$$\Rightarrow v_s = \left[\frac{R_S g_m}{1 + R_S g_m}\right] v_g$$

$\Rightarrow$ "follows" for $R_S \gg 1/g_m$

Note that source follower's $R_{out} = \frac{1}{g_m}$,

typically a few hundred ohms at $I_D \sim$ few milliamps.

Note also that bias network is less trivial for MOSFET (as in lab):



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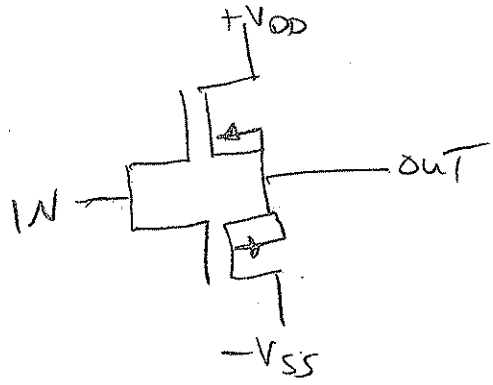
note ∃ "linear" region of I_D vs. V_{DS}

$$\frac{I_D}{V_{DS}} = \frac{1}{R_{DS}} = 2k\left[(V_{GS} - V_T) - \frac{V_{DS}}{2}\right]$$

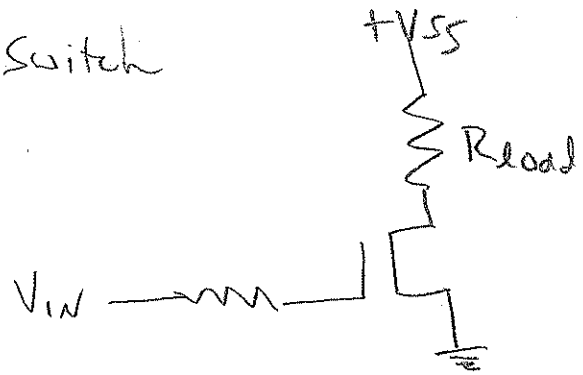
which (for small V_{DS}) allows FET to be used as a variable resistor.

We'll exploit this on Thursday.

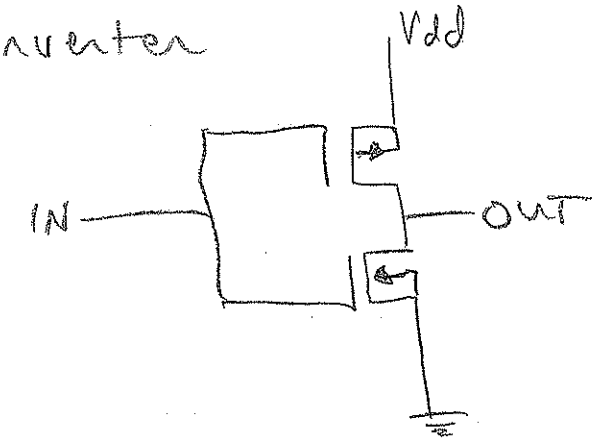
CMOS push-pull follower: (lab part 3)



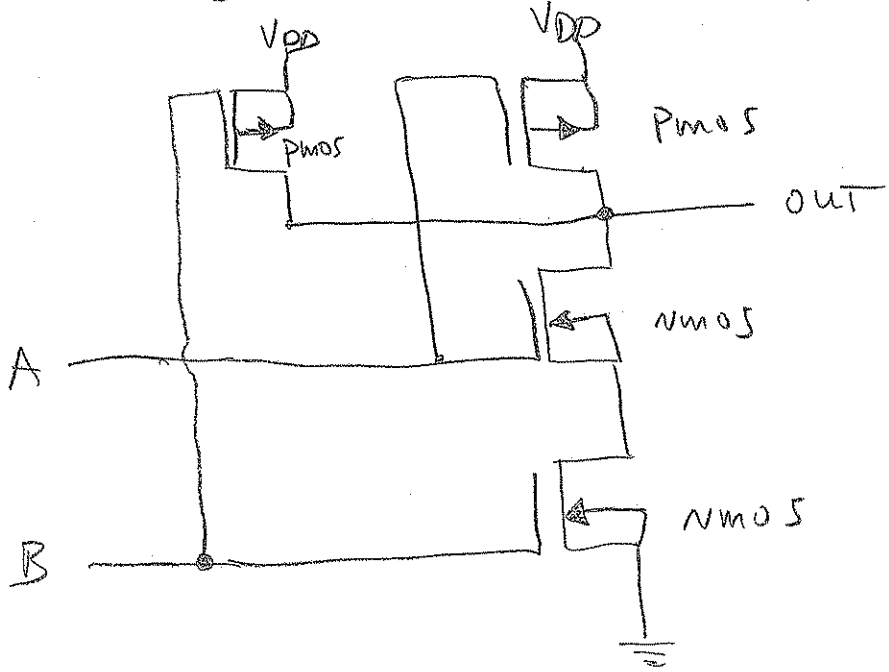
NMOS switch (lab part 4)



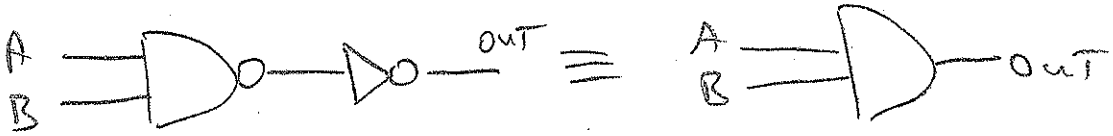
CMOS inverter (lab part 5)



CMOS NAND gate (lab part 6)



A	B	OUT
0	0	1
1	0	0
0	1	0
0	0	0



$$\neg(A \wedge B) = (\neg A) \vee (\neg B)$$

$$\neg(A \vee B) = (\neg A) \wedge (\neg B)$$

de Morgan