

Lecture 8

Why digital?

- Many quantities inherently discontinuous (discrete)  
 e.g. your account balance at bank, the number of long-sleeved black jersey shirts you own, your birthday, ...
- Discretization permits perfect reproduction  $\Rightarrow$  noise immunity
- Often can state required precision and discretize to keep that precision
- Once in digital form, data can be readily manipulated in useful ways, e.g. digital signal processing. ~~in MATLAB like~~

Why binary?

- It's a sensible alternative to decimal!
- Easy: ON/OFF  
 TRUE/FALSE  
 OPEN/CLOSED  
 maximal/minimal

Binary numbers

	0	0	
	1	1	
	10	2	
	11	3	
addition	100	4	multiplication long division fixed point floating point
subtraction	101	5	
representing negative values:	110	6	
	111	7	
	1000	8	
		:	

(seldom)  $\times$   
 (often)  $\rightarrow$

sign, magnitude  
 two's complement

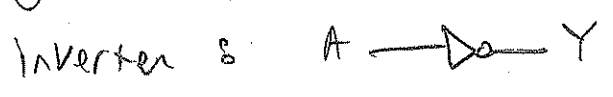
"bit" = "binary digit"

a string of  $N$  bits sometimes represents an integer  $0 \leq i < 2^N$ , sometimes a signed, fixed-point, or floating-point number, or sometimes represents  $N$  logical truth values.

bit = 0, 1  
 bit = FALSE, TRUE  
 bit = GROUND, VCC (LOW, HIGH)

logic gates

A	Y
0	1



$Y = \bar{A}$   
 (NOT A)  
 $\neg A, \neg A$

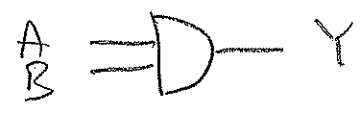
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1



$Y = A + B$   
 $A \parallel B$   
 $A \text{ OR } B$   
 $A \vee B$

AND (conjunction)

A	B	Y
0	0	0
0	1	0
1	0	0
1	1	1



$Y = AB$ ,  $A \cdot B$   
 $A \&\& B$   
 $A \text{ AND } B$   
 $A \wedge B$

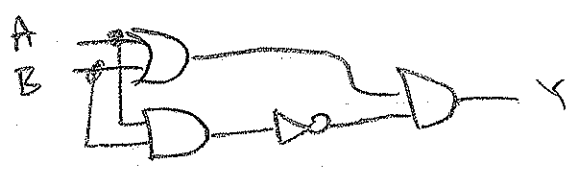
XOR (exclusive OR)

A	B	Y
0	0	0
0	1	1
1	0	1
1	1	0



$Y = A \oplus B$   
 $A \sim B$   
 $A \text{ XOR } B$   
 $A \neq B$

$(A \text{ XOR } B) = (A \text{ OR } B) \text{ AND NOT } (A \text{ AND } B)$

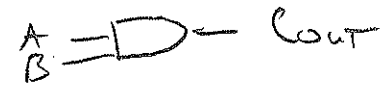
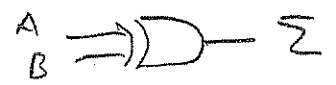


### 1-bit adder

A	B	$\Sigma$	Carryout
0	0	0	0
0	1	1	0
1	0	1	0
1	1	0	1

$$\Sigma = A \text{ XOR } B$$

$$\text{Carry} = A \text{ AND } B$$

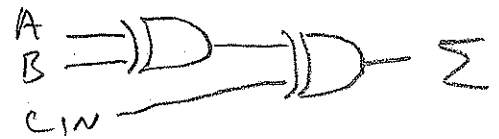


### 1-bit full adder

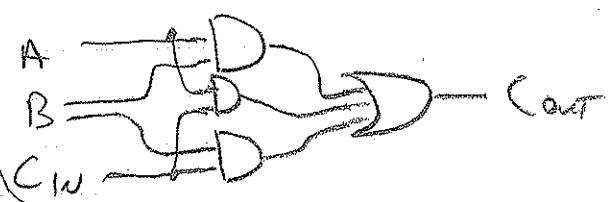
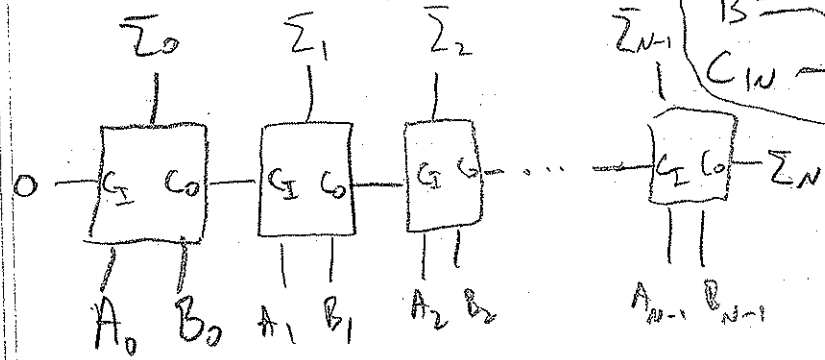
$C_{in}$	A	B	$C_{out}$	$\Sigma$
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

$$\Sigma = (A \text{ XOR } B) \text{ XOR } C_{in}$$

$$\text{Carry} = AB \text{ OR } AC_{in} \text{ OR } BC_{in}$$



add two N-bit numbers  $\rightarrow$  (N+1)-bit sum



### Multiplexer ("mux")

A <sub>1</sub>	A <sub>0</sub>	D <sub>3</sub>	A <sub>2</sub>	D <sub>1</sub>	D <sub>0</sub>	OUT
0	0					D <sub>0</sub>
0	1					D <sub>1</sub>
1	0					D <sub>2</sub>
1	1					D <sub>3</sub>

(choose one of N inputs to copy to output)

### Demultiplexer ("demux")

A <sub>1</sub>	A <sub>0</sub>	D	OUT <sub>3,2,1,0</sub>
0	0	D	0 0 0 D
0	1	D	0 0 D 0
1	0	D	0 D 0 0
1	1	D	D 0 0 0

(choose one of N outputs to which to copy input)

(Forgot to include priority encoder.)

### Other sorts of logic output :

- "Open collector" (also "open drain") :
  - logic 0 ⇒ ground
  - logic 1 ⇒ floating (high impedance)

### "tri-state" (or "three-state")

possible output states are { 0, 1, high impedance }  
 like "yes," "no," and (not speaking)

→ can create a sort of "party line" telephone — called a "bus"

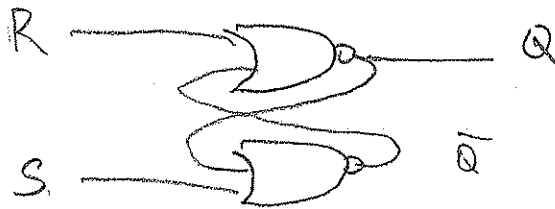
many senders can take turns driving data onto the bus

All of the above was "combinational" (sometimes called "combinatorial") logic — the present output reflects some combination of the present inputs.

It remembers nothing. Past inputs are irrelevant.

Suppose you want to store information for later use. Need a device with internal state, i.e. present inputs alone insufficient to determine output.

Consider this weird arrangement of NOR gates:



<u>S</u>	<u>R</u>	<u>Q</u>
0	1	0
1	0	1
0	0	Q <sub>previous</sub> (!)
1	1	0 (usually considered illegal input)

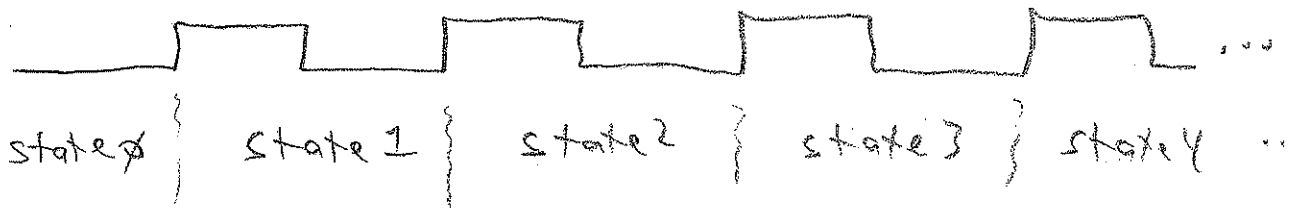
called a flip-flop (or a "bistable multivibrator" if you're feeling encyclopedic)

It can remember stored input!  
A one-bit memory.

Once your components can have an internal state, it's helpful to have a mechanism to get many of them to change state in concert — like the conductor of an orchestra, or a drum beat for marching troops, or the high school bell to signal the change of classrooms.

In sequential logic, this drumbeat role is played by the clock.

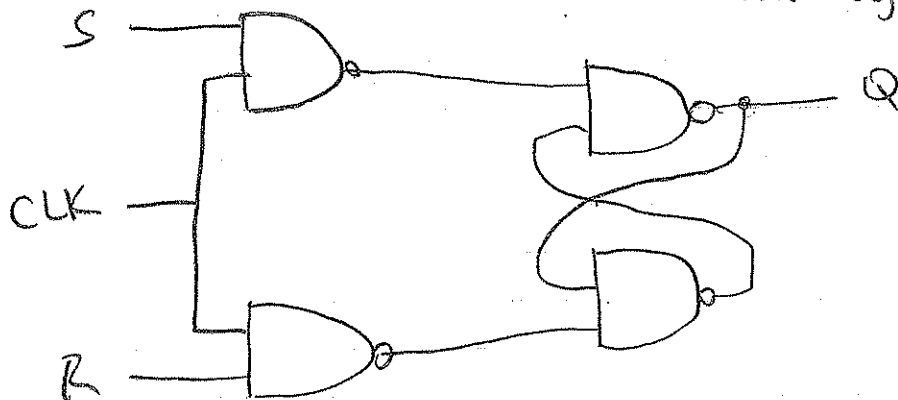
Typically, everybody agrees to change state on the rising edge of the clock.



How do you design a flip-flop to do that?

Here's a start (not quite satisfactory):

[Problem is that CLK is level-sensitive rather than edge-sensitive.]

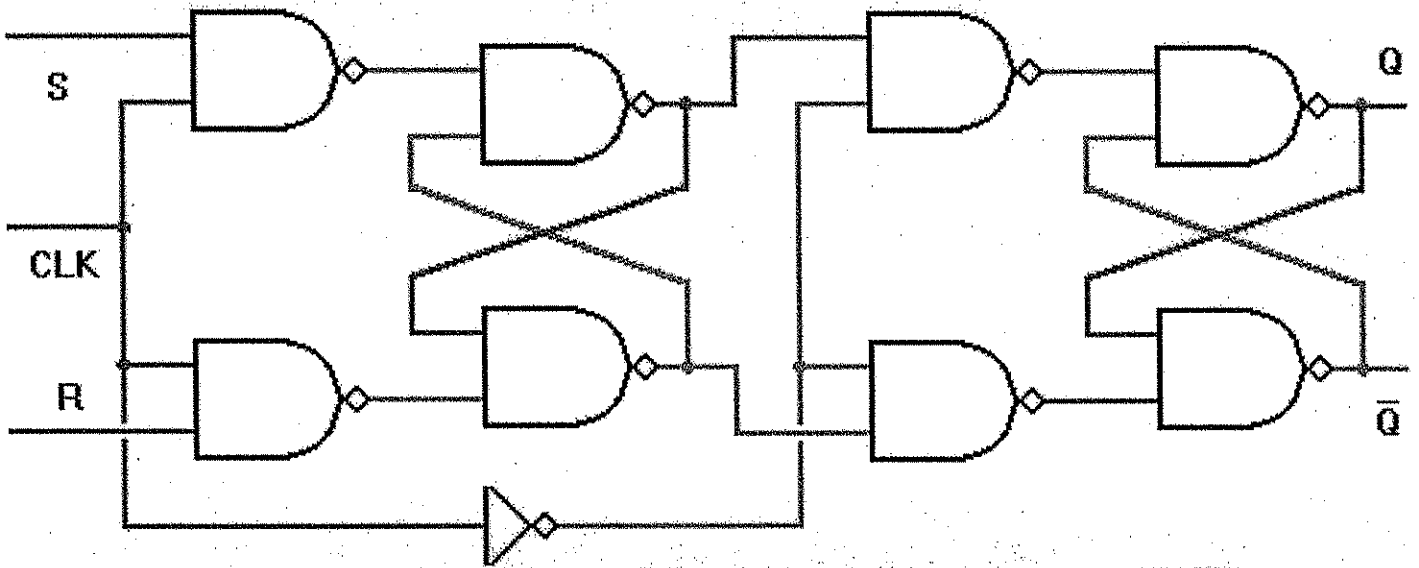


see [www.play-hokey.com/digital/clocked\\_rs\\_latch.html](http://www.play-hokey.com/digital/clocked_rs_latch.html)

[See animations at [www.play-hookey.com/digital](http://www.play-hookey.com/digital)]

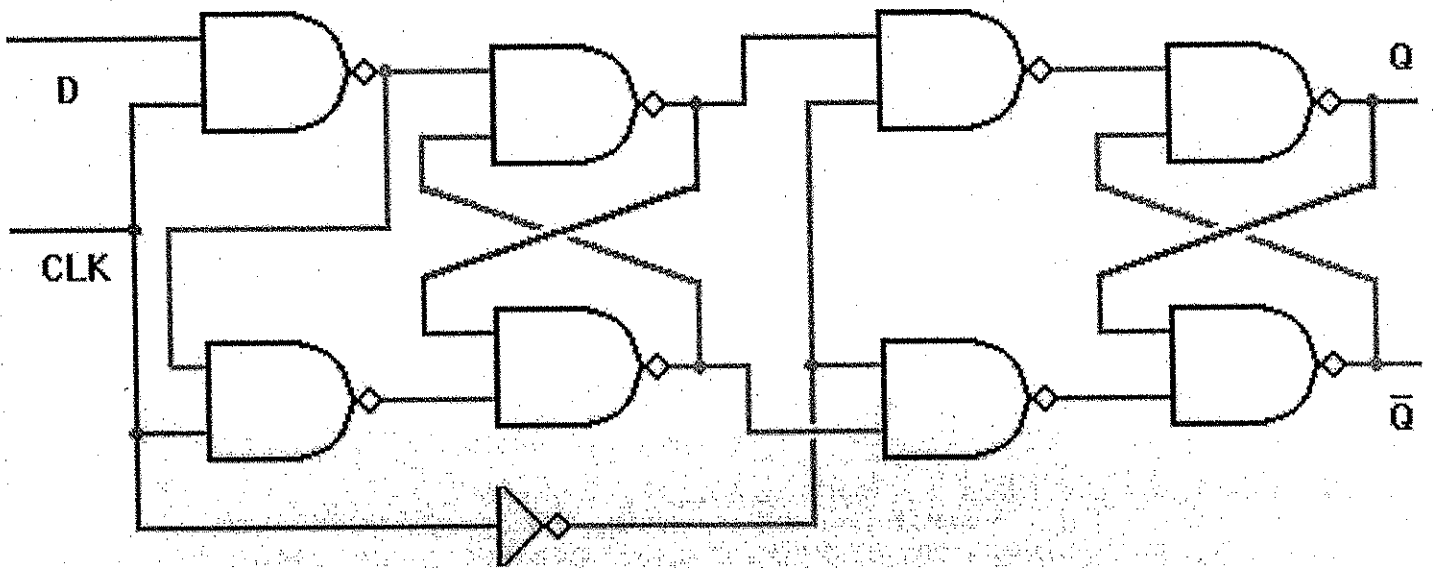
7

Somewhat better — records SR values at clock edge.





Called "master - slave" flip flop.

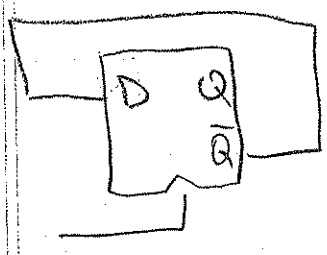
The most common FF is D-flop  
(vs. less common SR-flop, JK-flop, T-flop, ...)



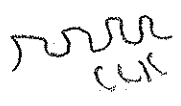
each clock cycle, Q reflects value of D on previous clock cycle.

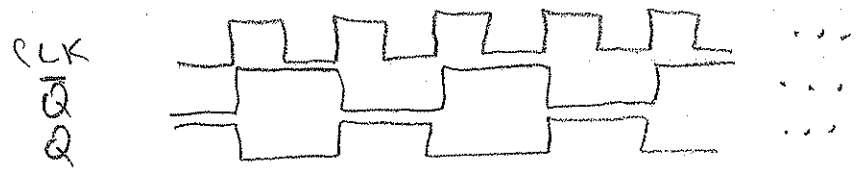
D-type  
In a real flip-flop, the change of Q is synchronous to the leading edge of CLK.

Q changes immediately after  and reflects state D had immediately before 

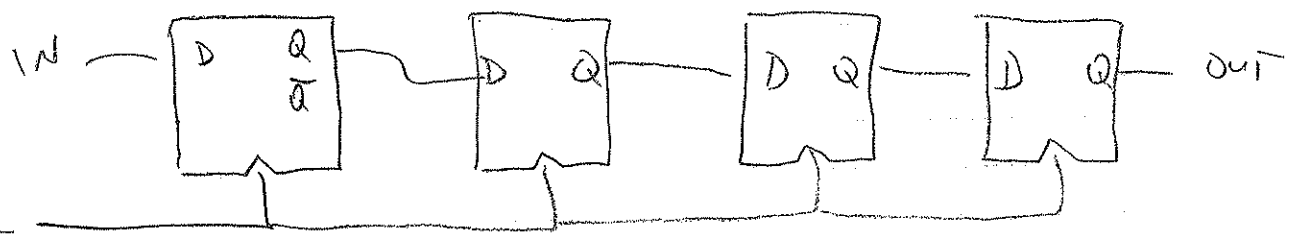


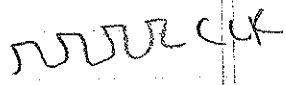
what does this do?

 CLK



sometimes called "divide by 2"



 CLK

This is a "pipeline"

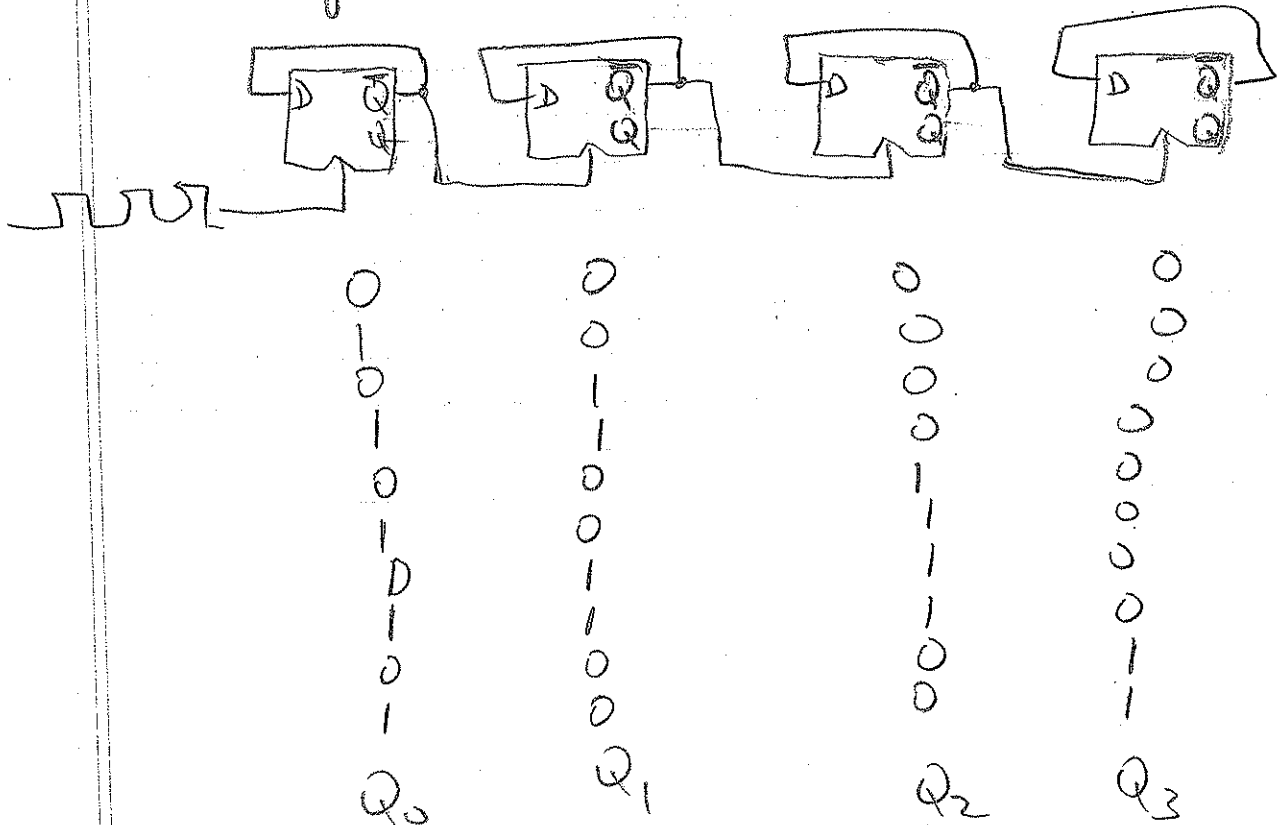
Like a fire fighter's bucket hand-off or a factory assembly line.

This particular pipeline is a "shift register"

(illustrate)

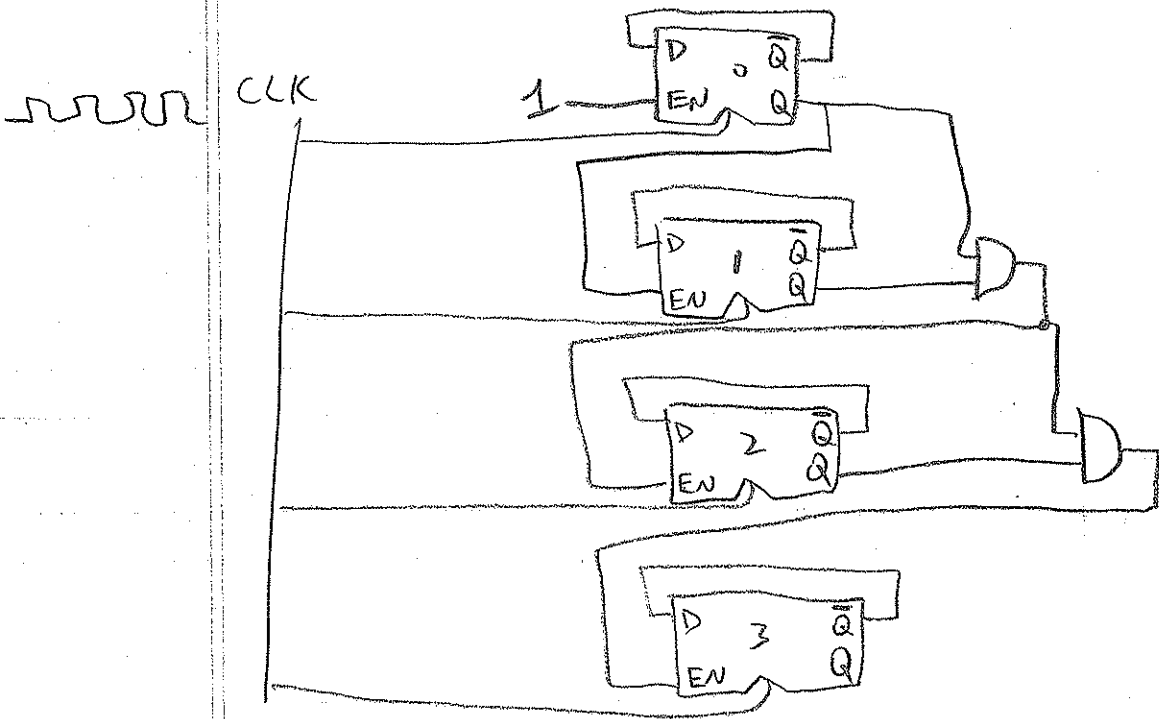


A "counter" is an often-seen circuit in sequential logic:



This "ripple clock" is not a good clock heard as the drum beat is not simultaneously by everyone.

[www.play-hokey.com/digital/ripple-counter.html](http://www.play-hokey.com/digital/ripple-counter.html)



Q <sub>3</sub>	Q <sub>2</sub>	Q <sub>1</sub>	Q <sub>0</sub>
0	0	0	0
0	0	0	1
0	0	1	0
0	0	1	1
0	1	0	0
0	1	0	1
0	1	1	0
0	1	1	1
1	0	0	0
1	0	0	1

etc.

Synchronous count  
every bit update  
at same  
clock edge.

# LAB 8 (early draft!)

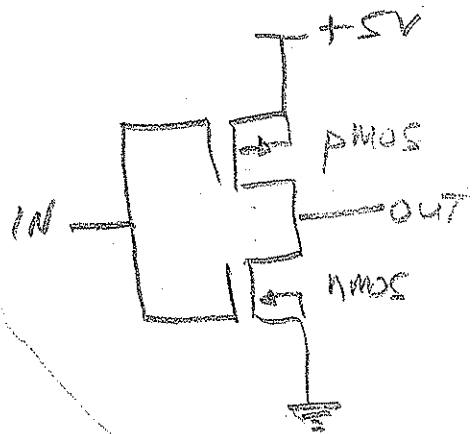
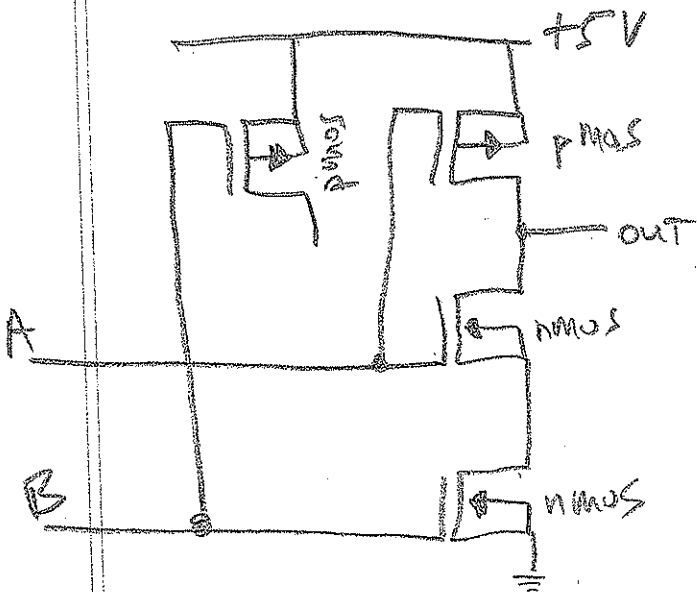
## ~~CMOS~~ NAND

Recall the CMOS inverter and NAND gate you built or simulated last week. Nearly all real-world logic nowadays is CMOS-based. But it turns out, to my surprise, that all discrete logic components currently available in the fab are ~~the~~ of the older TTL style (using BJTs), so we will spend this week working with TTL gates.

Partly this will give you a chance to learn a bit about the innards of logic gates; partly it will give you time to get well to the concepts; and partly it will illustrate for you what a terrific invention programmable logic is (FPGAs, etc.) ~~is~~ (i.e. tedious)

Recall CMOS inverter

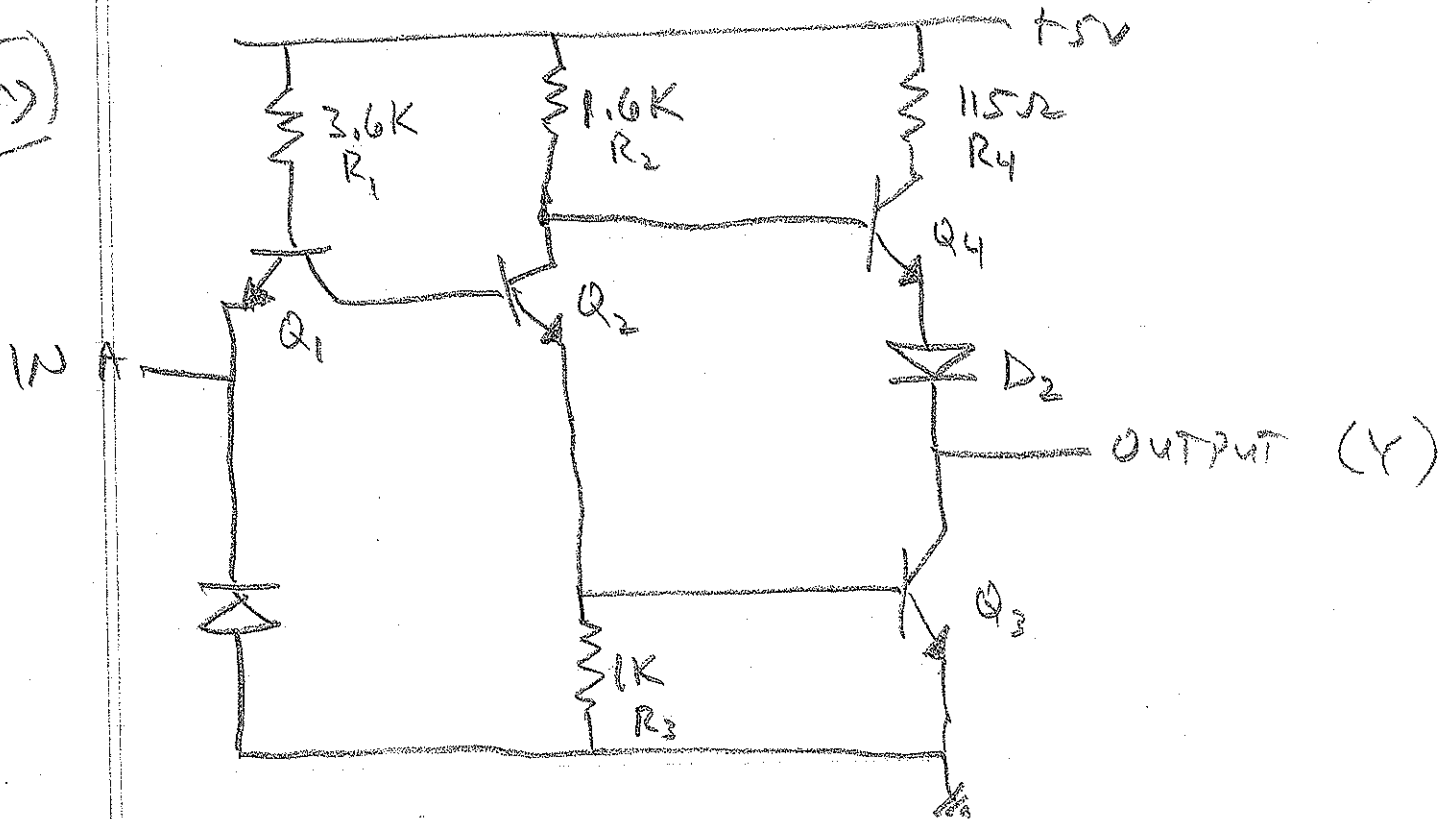
and CMOS NAND gate



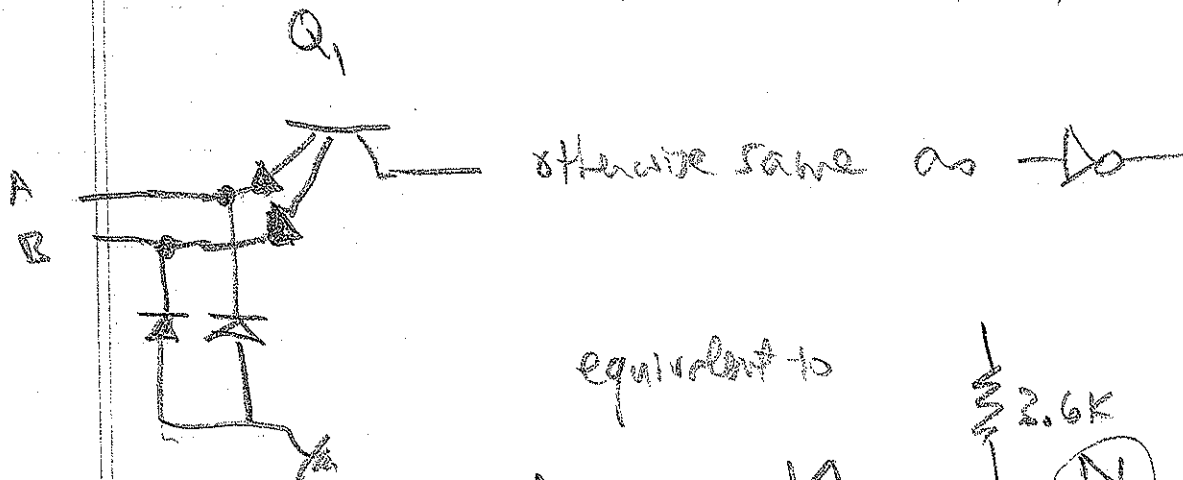
① check this out in SP3 RE

TTL inverter (7404 — somewhat different from 746504)

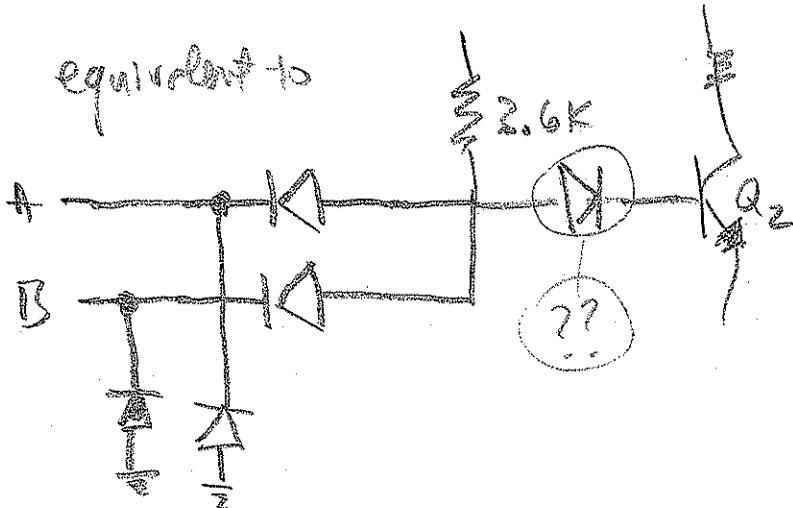
12.7.13



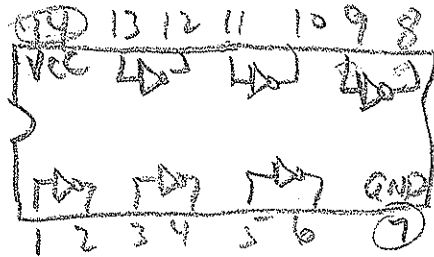
TTL NAND (7400)



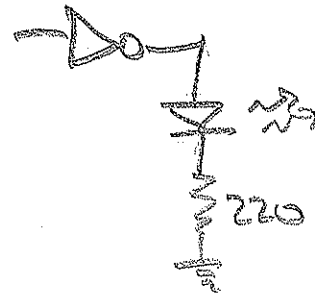
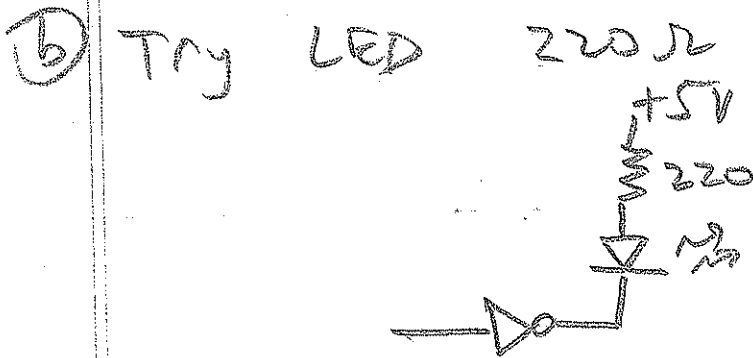
equivalent to



② Now get used to TTL inverter  
74LS04

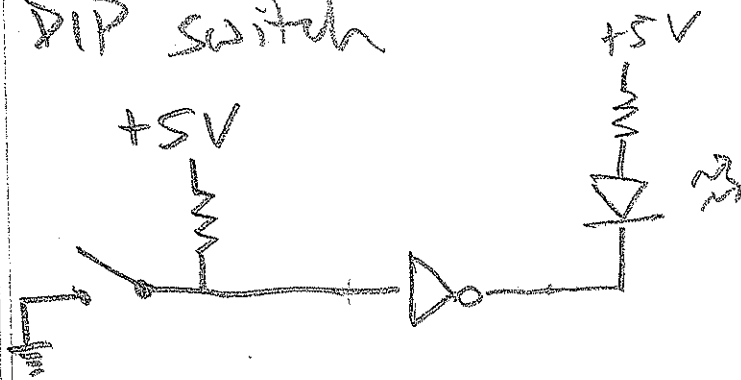


Connect VCC & gnd. Measure pin #2 vout vs. pin #1 vin, not exceeding +5V !! Where is threshold?

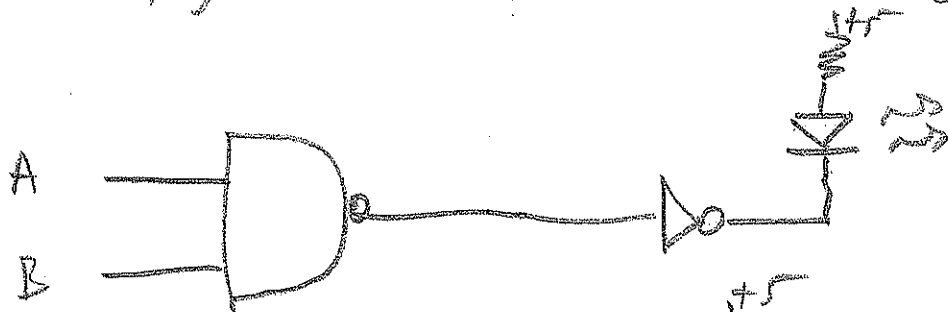


Which is brighter? Measure (or infer) current both ways.

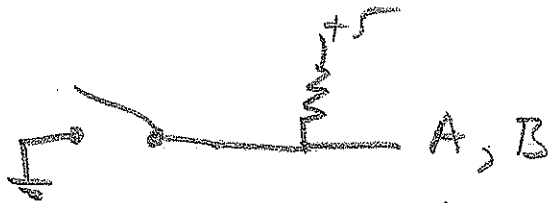
④ DIP switch



③ Now use your DIP switch (two inputs) and LED (with inverter) to try out 74LS00 NAND gate



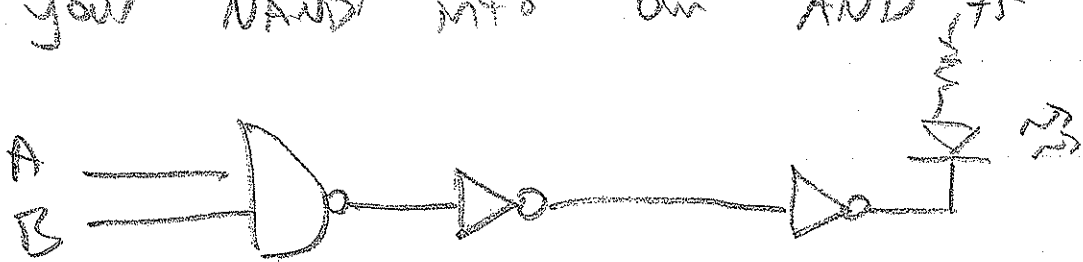
where



are driven by two DIP switches.

Write out logic table.

④ Use a spare inverter to make your NAND into an AND gate



⑤ Now use a 74LS08 AND instead.

⑥ Try 74LS32 OR now.

⑦ Try 74LS86 XOR now.

④ Check out the 74LS83  
4-bit binary full adder.

Prove to yourself that it  
correctly adds two 4-bit numbers  
together.

How would you build such an  
adder from discrete gates  
(AND, OR, XOR, inverters, etc.)?

(Draw only — don't build it!)  
Don't forget  $C_{in}$ ,  $C_{out}$ !

⑤ Try a 74LS138 decoder!

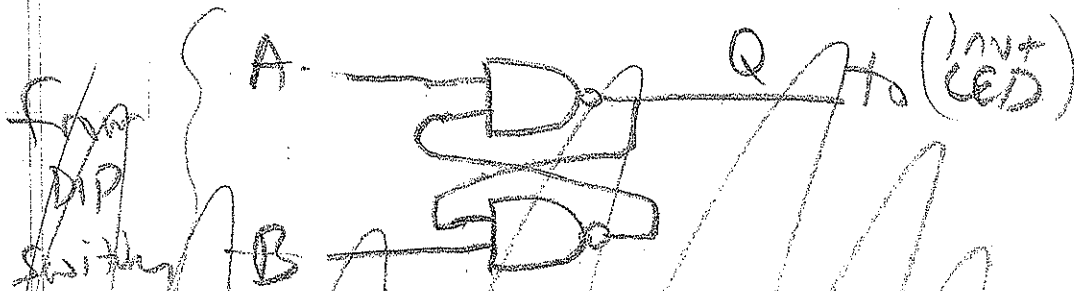
$E_1, E_2 \rightarrow GND$  ;  $E_3 \rightarrow VCC$

use DIP to control  $A_0, A_1, A_2$

display  $\bar{O}_0 \rightarrow \bar{O}_7$  on LEDs.

For added fun, make  $E_3$  oscillate as  
a 1 Hz TTL pulse from function  
generator (careful with voltage levels).

primitive flip-flop



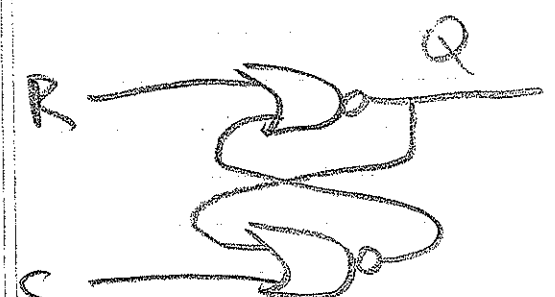
from DP switch

A	B	Q
0	0	1
0	1	0
1	0	0
1	1	Q

(sort of forbidden)

Notice that set\* while A acts as an active-low reset\* with B acts as an active-low deasserted, and both (active) inputs remember its old value!

from DP switch



7402 NOR

R	S	Q
0	0	1
0	1	0
1	0	0
1	1	(forbidden / 0)

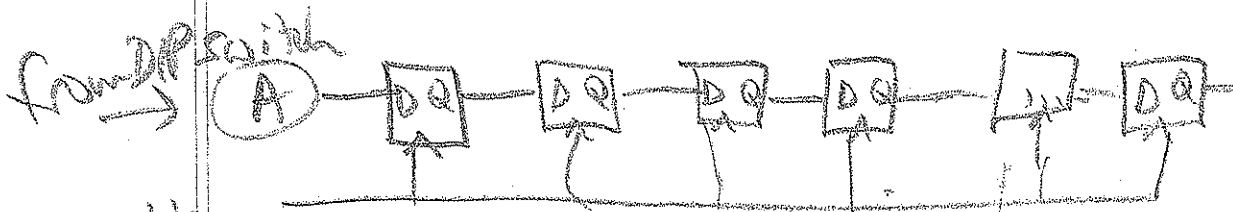
[ See [www.play-hookey.com/digital/d-nor-flip-flop.html](http://www.play-hookey.com/digital/d-nor-flip-flop.html) ]



⑦ Useful ner of clock: like the conductor of an orchestra, or the change-of class bell in a high school — tells everyone to change state at the same time.

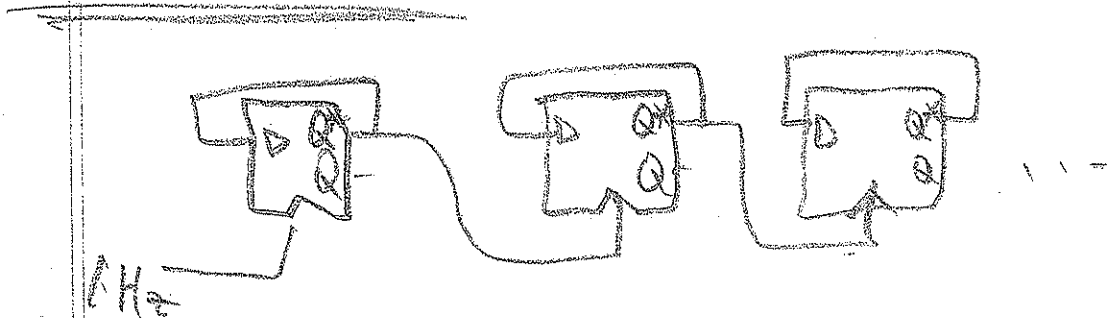
Having a memory (hence statefulness) and having a clock (for coordinating changes of state) often go together.

74LS74 dual DFF (2 of them)



CLK  
1Hz  
TTL

Send all 6 Q's to your inputs/LED outputs.



notice that each successive Q counts at half the speed of the previous.

"Ripple clock" (bad design, actually, as we no longer have a single drummer)

⑧ Try 74LS 164 8-bit shift register  
with same setup.

Try 74LS 169 4-bit counter,  
with 1Hz clock, displaying to  
4 LEDs

⑨ One of the few metal discrete!  
a one-shot

74121 (74LS 121 ?)