PHYSICS 364, fall 2010

For Week 4:

- read my notes and the ✓'ed sections from Horowitz & Hill on advanced opamp topics & comparators. Ignore X'ed sections.

  My notes will be completed tomorrow — first 8 pages are attached here.

  Do reading in time for Monday lecture, 2010-10-04.

- Solve the attached opamp homework problems from Prof. Krall.
  Due by Thursday lab, 2010-10-07.

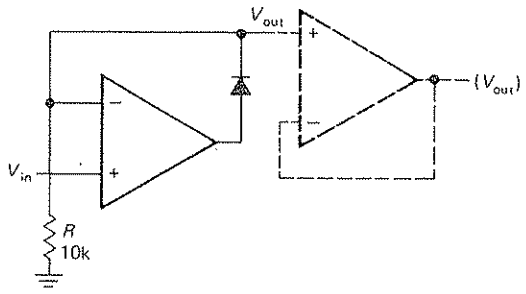

Figure 4.25. Simple active rectifier.

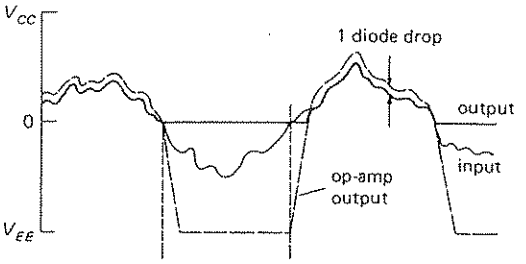

Figure 4.26. Effect of finite slew rate on the simple active rectifier.

There is a problem with this circuit that becomes serious with high-speed signals. Because an op-amp cannot swing its output infinitely fast, the recovery from negative saturation (as the input waveform passes through zero from below) takes some time, during which the output is incorrect. It looks something like the curve shown in Figure 4.26. The output (heavy line) is an accurate rectified version of the input (light line), except for a short time interval after the input rises through zero volts. During that interval the op-amp output is racing up from saturation near $-V_{EE}$, so the circuit's output is still at ground. A general-purpose op-amp like the 411 has a *slew rate* (maximum rate at which the output can change) of 15 volts per microsecond; recovery from negative saturation therefore takes about 1μs, which may introduce significant output error for fast signals. A circuit modification improves the situation considerably (Fig. 4.27).

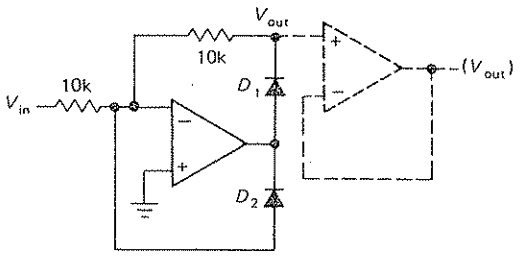

Figure 4.27. Improved active rectifier.

D_1 makes the circuit a unity-gain inverter for negative input signals. D_2 clamps the op-amp's output at one diode drop below ground for positive inputs, and since D_1 is then back-biased, V_{out} sits at ground. The improvement comes because the op-amp's output swings only two diode drops as the input signal passes through zero. Since the op-amp output has to slew only about 1.2 volts instead of V_{EE} volts, the "glitch" at zero crossings is reduced more than tenfold. This rectifier is inverting, incidentally. If you require a noninverted output, attach a unity-gain inverter to the output.

The performance of these circuits is improved if you choose an op-amp with a high slew rate. Slew rate also influences the performance of the other op-amp applications we've discussed, for instance the simple voltage amplifier circuits. At this point it is worth pausing for a while to see in what ways real op-amps depart from the ideal, since that influences circuit design, as we have hinted on several occasions. A good understanding of op-amp limitations and their influence on circuit design and performance will help you choose your op-amps wisely and design with them effectively.

A DETAILED LOOK AT OP-AMP BEHAVIOR

Figure 4.28 shows the schematic of the 741, a very popular op-amp. Its circuit is

relatively straightforward, in terms of the kinds of transistor circuits we discussed in the last chapter. It has a differential input stage with current mirror load, followed by a common-emitter *npn* stage (again with active load) that provides most of the voltage gain. A *pnp* emitter follower drives the push-pull emitter follower output stage, which includes current-limiting circuitry. This circuit is typical of many op-amps now available. For many applications the properties of these amplifiers approach ideal op-amp performance characteristics. We will now take a look at the extent to which real op-amps depart from the ideal, what the consequences are for circuit design, and what to do about it.

4.11 Departure from ideal op-amp performance

The ideal op-amp has these characteristics:

1. Input impedance (differential or common mode) = infinity
2. Output impedance (open loop) = 0
3. Voltage gain = infinity
4. Common-mode voltage gain = 0
5. $V_{out} = 0$ when both inputs are at the same voltage (zero "offset voltage")
6. Output can change instantaneously (infinite slew rate)

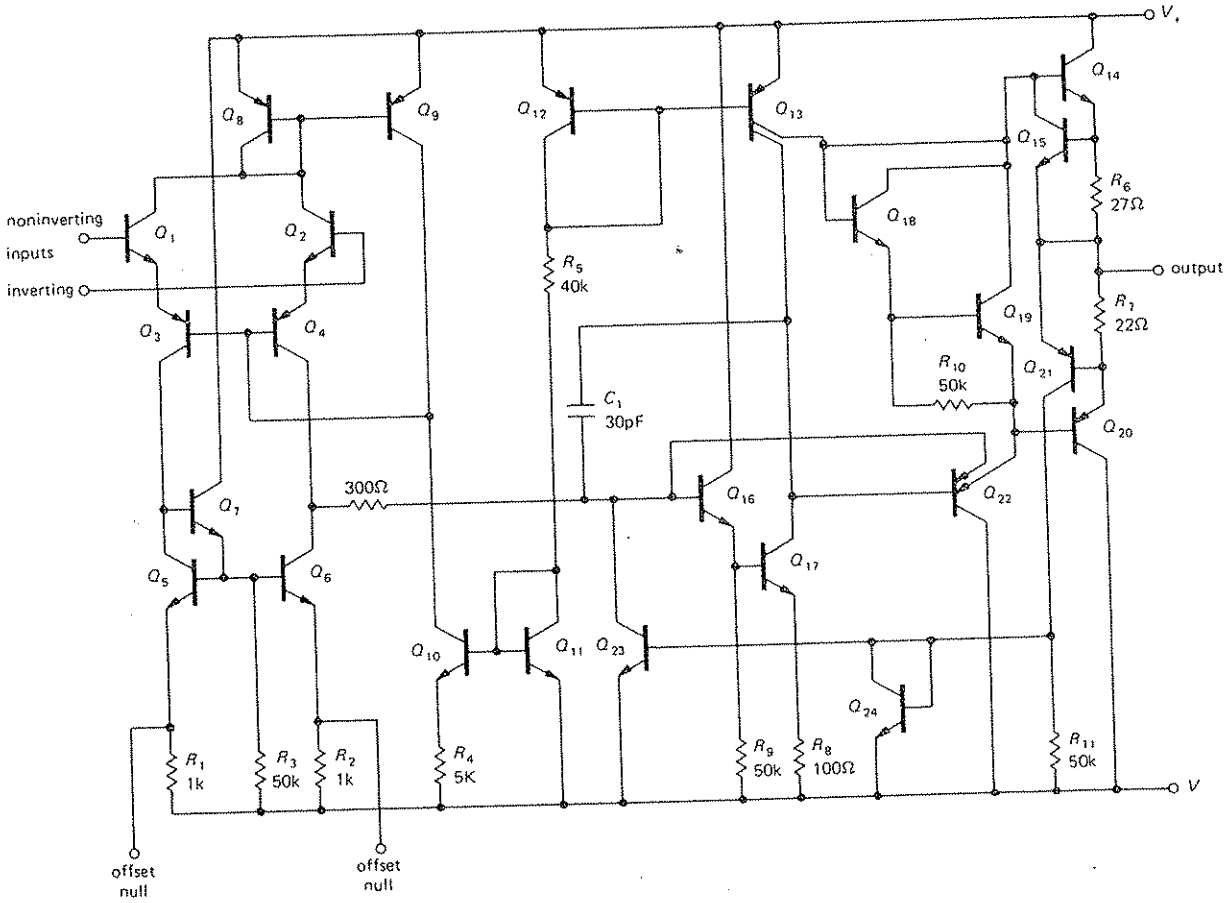

Figure 4.28. Schematic of the 741 op-amp. (Courtesy of Fairchild Camera and Instrument Corp.)

All of these characteristics are independent of temperature and supply voltage changes.

Real op-amps depart from these characteristics in the following ways (see Table 4.1 for some typical values).

Input current

The input terminals sink (or source, depending on the op-amp type) a small current called the input bias current, I_B, which is defined as half the sum of the input currents with the inputs tied together (the two input currents are approximately equal and are simply the base or gate currents of the input transistors). For the JFET-input 411 the bias current is typically 50pA at room temperature (but as much as 2nA at 70°C), while a typical BJT-input op-amp like the OP-27 has a typical bias current of 15nA, varying little with temperature. As a rough guide, BJT-input op-amps have bias currents in the tens of nanoamps, while FET-input op-amps have input currents in the tens of picoamps (i.e., 1000 times lower). Generally speaking, you can ignore input current with FET op-amps, but not with bipolar-input op-amps.

The significance of input bias current is that it causes a voltage drop across the resistors of the feedback network, bias network, or source impedance. How small a resistor this restricts you to depends on the dc gain of your circuit and how much output variation you can tolerate. You will see how this works later.

Op-amps are available with input bias currents down to a nanoamp or less for (bipolar) transistor-input circuit types or down to a few picoamps ($10^{-6}\mu$A) for FET-input circuit types. The very lowest bias currents are typified by the superbeta Darlington LM11, with a maximum input current of 50pA, the AD549, with an input current of 0.06pA, and the MOSFET ICH8500, with an input current of 0.01pA. In general, transistor op-amps intended for high-speed operation have higher bias currents.

Input offset current

Input offset current is a fancy name for the difference in input currents between the two inputs. Unlike input bias current, the offset current, I_{os}, is a result of manufacturing variations, since an op-amp's symmetrical input circuit would otherwise result in identical bias currents at the two inputs. The significance is that even when it is driven by identical source impedances, the op-amp will see unequal voltage drops and hence a difference voltage between its inputs. You will see shortly how this influences design.

Typically, the offset current is one-half to one-tenth the bias current. For the 411, $I_{\text{offset}} = 25$pA, typical.

☐ *Input impedance*

Input impedance refers to the differential input resistance (impedance looking into one input, with the other input grounded), which is usually much less than the common-mode resistance (a typical input stage looks like a long-tailed pair with current source). For the FET-input 411 it is about 10^{12} ohms, while for BJT-input op-amps like the 741 it is about 2MΩ. Because of the input bootstrapping effect of negative feedback (it attempts to keep both inputs at the same voltage, thus eliminating most of the differential input signal), Z_{in} in practice is raised to very high values and usually is not as important a parameter as input bias current.

☐ *Common-mode input range*

The inputs to an op-amp must stay within a certain voltage range, typically less than the full supply range, for proper operation. If the inputs go beyond this range, the gain of the op-amp may change drastically, even reversing sign! For a 411 operating

from ±15 volt supplies, the guaranteed common-mode input range is ±11 volts minimum. However, the manufacturer claims that the 411 will operate with common-mode inputs all the way to the positive supply, though performance may be degraded. Bringing either input down to the negative supply voltage causes the amplifier to go berserk, with symptoms like phase reversal and output saturation to the positive supply.

There are op-amps available with common-mode input ranges down to the negative supply, e.g., the LM358 (a good dual op-amp) or the LM10, CA3440, or OP-22, and up to the positive supply, e.g., the 301, OP-41, or the 355 series. In addition to the *operating* common-mode range, there are maximum allowable input voltages beyond which damage will result. For the 411 they are ±15 volts (but not to exceed the negative supply voltage, if it is less).

Differential input range

Some bipolar op-amps allow only a limited voltage between the inputs, sometimes as small as ±0.5 volt, although most are more forgiving, permitting differential inputs nearly as large as the supply voltages. Exceeding the specified maximum can degrade or destroy the op-amp.

☐ *Output impedance; output swing versus load resistance*

Output impedance R_0 means the op-amp's intrinsic output impedance *without feedback*. For the 411 it is about 40 ohms, but with some low-power op-amps it can be as high as several thousand ohms (see Fig. 7.16). Feedback lowers the output impedance into insignificance (or raises it, for a current source); so what usually matters more is the maximum output current, with typical values of 20mA or so. This is frequently given as a graph of output voltage swing V_{om} as a function of load resistance, or sometimes just a few values for typical load resistances. Many op-amps have asymmetrical output drive capability, with the ability to sink more current than they can source (or vice versa). For the 411, output swings to within about 2 volts of V_{CC} and V_{EE} are possible into load resistances greater than about 1k. Load resistances significantly less than that will permit only a small swing. Some op-amps can produce output swings all the way down to the negative supply (e.g., the LM358), a particularly useful feature for circuits operated from a single positive supply, since output swings all the way to ground are then possible. Finally, op-amps with MOS transistor outputs (e.g., the CA3130, 3160, ALD1701, and ICL761x) can swing all the way to both rails. The remarkable bipolar LM10 shares this property, without the limited supply voltage range of the MOS op-amps (usually ±8V max).

☐ *Voltage gain and phase shift*

Typically the voltage gain A_{vo} at dc is 100,000 to 1,000,000 (often specified in decibels), dropping to unity gain at a frequency (called f_T) of 1MHz to 10MHz. This is usually given as a graph of open-loop voltage gain as a function of frequency. For *internally compensated* op-amps this graph is simply a 6dB/octave rolloff beginning at some fairly low frequency (for the 411 it begins at about 10Hz), an intentional characteristic necessary for stability, as you will see in Section 4.32. This rolloff (the same as a simple RC low-pass filter) results in a constant 90° lagging phase shift from input to output (open-loop) at all frequencies above the beginning of the rolloff, increasing to 120° to 160° as the open-loop gain approaches unity. Since a 180° phase shift at a frequency where the voltage gain equals 1 will result in positive feedback (oscillations), the term "phase margin" is used to specify the difference between the phase shift at f_T and 180°.

Input offset voltage

Op-amps don't have perfectly balanced input stages, owing to manufacturing variations. If you connect the two inputs together for zero input signal, the output will usually saturate at either V_{CC} or V_{EE} (you can't predict which). The difference in input voltages necessary to bring the output to zero is called the input offset voltage V_{os} (it's as if there were a battery of that voltage in series with one of the inputs). Usually op-amps make provision for trimming the input offset voltage to zero. For a 411 you use a 10k pot between pins 1 and 5, with the wiper connected to V_{EE}.

Of greater importance for precision applications is the drift of the input offset voltage with temperature and time, since any initial offset can be trimmed to zero. A 411 has a typical offset voltage of 0.8mV (2mV maximum), with temperature coefficient ("tempco") of 7μV/°C and unspecified coefficient of offset drift with time. The OP-77, a precision op-amp, is laser-trimmed for a typical offset of 10 *microvolts*, with temperature coefficient TCV_{os} of 0.2μV/°C and long-term drift of 0.2μV/month.

Slew rate

The op-amp "compensation" capacitance (discussed further in Section 4.32) and small internal drive currents act together to limit the rate at which the output can change, even when a large input unbalance occurs. This limiting speed is usually specified as *slew rate* or slewing rate (SR). For the 411 it is 15V/μs; low-power op-amps typically have slew rates less than 1V/μs, while a high-speed op-amp might slew at 100V/μs, and the LH0063C "damn fast buffer" slews at 6000V/μs. The slew rate limits the amplitude of an undistorted sine-wave output swing above some critical frequency (the frequency at which the full supply swing requires the maximum slew rate of the op-amp, Fig. 4.29), thus explaining the "output voltage swing as a function of frequency" graph. A sine wave of frequency f hertz and amplitude A volts requires a minimum slew rate of $2\pi Af$ volts per second.

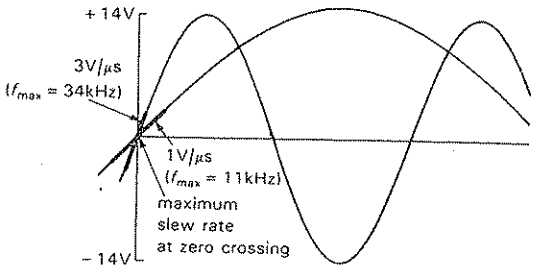

Figure 4.29. Slew-rate-induced distortion.

For externally compensated op-amps the slew rate depends on the compensation network used. In general, it will be lowest for "unity gain compensation," increasing to perhaps 30 times faster for ×100 gain compensation. This is discussed further in Section 4.32.

Temperature dependence

All these parameters have some temperature dependence. However, this usually doesn't make any difference, since small variations in gain, for example, are almost entirely compensated by feedback. Furthermore, the variations of these parameters with temperature are typically small compared with the variations from unit to unit.

The exceptions are input offset voltage and input offset current. This will matter, particularly if you've trimmed the offsets approximately to zero, and will appear as drifts in the output. When high precision is important, a low-drift "instrumentation" op-amp should be used, with external loads kept above 10k to minimize

the horrendous effects on input-stage performance caused by temperature gradients. We will have much more to say about this subject in Chapter 7.

For completeness, we should mention here that op-amps are also limited in common-mode rejection ratio (CMRR), power-supply rejection ratio (PSRR), input noise voltage and current (e_n, i_n), and output crossover distortion. These become significant limitations only in connection with precision circuits and low-noise amplifiers, and they will be treated in Chapter 7.

4.12 Effects of op-amp limitations on circuit behavior

Let's go back and look at the inverting amplifier with these limitations in mind. You will see how they affect performance, and you will learn how to design effectively in spite of them. With the understanding you will get from this example, you should be able to handle other op-amp circuits. Figure 4.30 shows the circuit again.

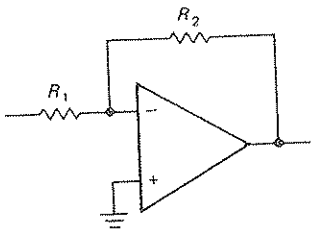

Figure 4.30

Open-loop gain

Because of finite open-loop gain, the voltage gain of the amplifier with feedback (closed-loop gain) will begin dropping at a frequency where the open-loop gain approaches R_2/R_1 (Fig. 4.31). For garden-variety op-amps like the 411, this means that you're dealing with a relatively low frequency amplifier; the open-loop gain is down to 100 at 50kHz, and f_T is 4MHz. Note that the closed-loop gain is always less than the open-loop gain; this means, for instance, that a $\times 100$ amplifier built with a 411 will show a noticeable falloff of gain for frequencies approaching 50kHz. Later in the chapter (Section 4.25), when we deal with transistor feedback circuits with finite open-loop gains, we will have a more accurate statement of this behavior.

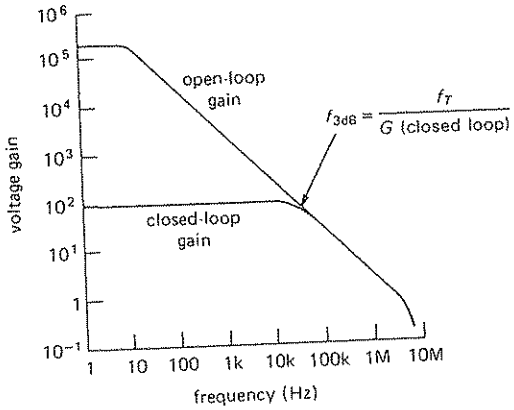

Figure 4.31. LF411 gain versus frequency ("Bode plot").

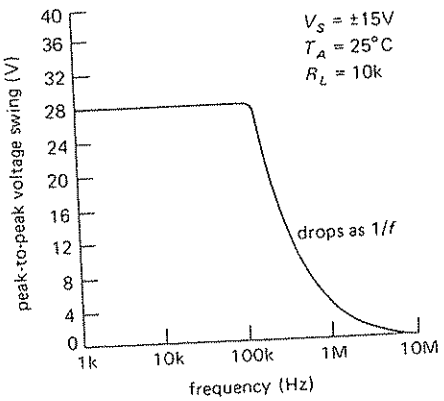

Figure 4.32. Output swing versus frequency (LF411).

Slew rate

Because of limited slew rate, the maximum undistorted sine-wave output swing drops above a certain frequency. Figure 4.32 shows the curve for a 411, with its 15V/μs

slew rate. For slew rate S, the output amplitude is limited to $A(\text{pp}) \leq S/\pi f$ for a sine wave of frequency f, thus explaining the $1/f$ dropoff of the curve. The flat portion of the curve reflects the power-supply limits of output voltage swing.

As an aside, the slew-rate limitation of op-amps can be usefully exploited to filter sharp noise spikes from a desired signal, with a technique known as *nonlinear low-pass filtering*. By deliberately limiting the slew rate, the fast spikes can be dramatically reduced without any distortion of the underlying signal.

Output current

Because of limited output current capability, an op-amp's output swing is reduced for small load resistances. Figure 4.33 shows the graph for a 411. For precision applications it is a good idea to avoid large output currents in order to prevent on-chip thermal gradients produced by excessive power dissipation in the output stage.

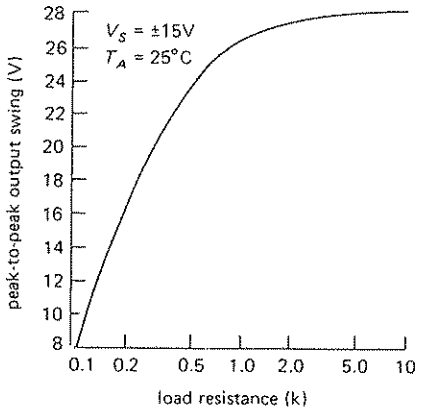

Figure 4.33. Output swing versus load (LF411).

Offset voltage

Because of input offset voltage, a zero input produces an output of $V_{\text{out}} = G_{dc}V_{os}$. For an inverting amplifier with voltage gain of 100 built with a 411, the output could be as large as ±0.2 volt when the input is grounded (V_{os} = 2mV max). Solutions: (a) If you don't need gain at dc, use a capacitor to drop the gain to unity at dc, as in Figure 4.7, as well as the RIAA amplifier circuit (Fig. 4.20). In this case you could do that by capacitively coupling the input signal. (b) Trim the voltage offset to zero using the manufacturer's recommended trimming network. (c) Use an op-amp with smaller V_{os}. (d) Trim the voltage offset to zero using an external trimming network as described in Section 7.06 (Fig. 7.5).

Input bias current

Even with a perfectly trimmed op-amp (i.e., $V_{os} = 0$), our inverting amplifier circuit will produce a non-zero output voltage when its input terminal is connected to ground. That is because the finite input bias current, I_B, produces a voltage drop across the resistors, which is then amplified by the circuit's voltage gain. In this circuit the inverting input sees a driving impedance of $R_1 \parallel R_2$, so the bias current produces a voltage $V_{\text{in}} = I_B(R_1 \parallel R_2)$, which is then amplified by the gain at dc, $-R_2/R_1$.

With FET-input op-amps the effect is usually negligible, but the substantial input current of bipolar op-amps can cause real problems. For example, consider an inverting amplifier with $R_1 = 10\text{k}$ and $R_2 = 1\text{M}$; these are reasonable values for an inverting stage, where we might like to keep Z_{in} at least 10k. If we chose the low-noise bipolar LM833, the output (for grounded input) could be as large as 100×1000nA×9.9k, or 0.99 volt ($G_{dc}I_B R_{\text{unbalance}}$), which is unacceptable. By comparison, for our jellybean LF411 (JFET-input) op-amp the corresponding worst-case output (for grounded input) is 0.2mV; for most applications this is negligible, and in any case is dwarfed by the

V_{os}-produced output error (200mV, worst-case untrimmed, for the LF411).

There are several solutions to the problem of bias-current errors. If you must use an op-amp with large bias current, it is a good idea to ensure that both inputs see the same dc driving resistance, as in Figure 4.34. In this case, 9.1k is chosen as the parallel resistance of 10k and 100k. In addition, it is best to keep the resistance of the feedback network small enough so that bias current doesn't produce large offsets; typical values for the resistance seen from the op-amp inputs are 1k to 100k or so. A third cure involves reducing the gain to unity at dc, as in the RIAA amplifier earlier.

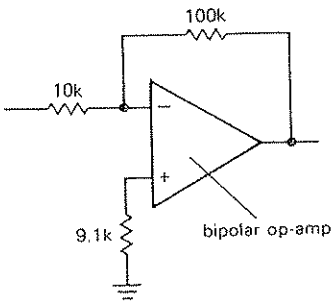

Figure 4.34. With bipolar op-amps, use a compensation resistor to reduce errors caused by input bias current.

In most cases, though, the simplest solution is to use op-amps with negligible input current. Op-amps with JFET or MOSFET input stages generally have input currents in the picoamp range (watch out for its rapid rise versus temperature, though, roughly doubling every 10°C), and many modern bipolar designs use superbeta transistors or bias-cancellation schemes to achieve bias currents nearly as low, *decreasing* slightly with temperature. With these op-amps, you can have the advantages of bipolar op-amps (precision, low noise) without the annoying problems caused by input current. For example, the precision low-noise bipolar OP-27 has I_B =10nA (typ), the inexpensive bipolar LM312 has I_B =1.5nA (typ), and its improved bipolar cousins (the LT1012 and LM11) have I_B = 30pA (typ). Among inexpensive FET op-amps, the JFET LF411 has I_B = 50pA (typ), and the MOSFET TLC270 series, priced under a dollar, have I_B = 1pA (typ).

Input offset current

As we just described, it is usually best to design circuits so that circuit impedances, combined with op-amp bias current, produce negligible errors. However, occasionally it may be necessary to use an op-amp with high bias current, or to deal with signals of extraordinarily high Thévenin impedances. In that case the best you can do is to balance the dc driving resistances seen by the op-amp at its input terminals. There will still be some error at the output ($G_{dc}I_{\text{offset}}R_{\text{source}}$), due to unavoidable asymmetry in the op-amp input currents. In general, I_{offset} is smaller than I_{bias} by a factor of 2 to 20 (with bipolar op-amps generally showing better matching than FET op-amps).

In the preceding paragraphs we have discussed the effects of op-amp limitations, taking the example of the simple inverting voltage amplifier circuit. Thus, for example, op-amp input current caused a *voltage* error at the output. In a different op-amp application you may get a different effect; for example, in an op-amp integrator circuit, finite input current produces an output *ramp* (rather than a constant) with zero applied input. As you become familiar with op-amp circuits you will be able to predict the effects of op-amp limitations in a given circuit and therefore choose which op-amp to use in a given application. In general, there is no "best" op-amp (even when price is no object): For example,

TABLE 4.2. RECOMMENDED OP-AMPS

Type	Mfg[a]	Amps per package[b] 1	2	4	Offset voltage max (mV)	Offset drift max (µV/°C)	Input curr max (nA)	Total supply voltage min (V)	Total supply voltage max (V)	Supply curr max (mA)	e_n, typ 10Hz (nV/√Hz)	e_n, typ 1kHz (nV/√Hz)	Slew rate typ (V/µs)	f_T typ (MHz)	Comments
LF411	NS	•	A	–	2	20	0.2	10	36	3.4	50	25	15	4	general purpose jellybean
AD711K	AD	•	A	–	0.5	10	0.05	9	36	3	45	18	20	4	improved LF411
LM358A	NS+	–	•	A	3	20	100	3	32	1.2	–	–	0.5	1	single supply jellybean
TLC27M2A	TI	A	•	A	5	2[t]	0.001[t]	3	18	0.6	–	–	0.6	0.7	CMOS jellybean
OP-27E	PM+	•	A	A	0.025	0.6	40	8	44	5	3.5	3.0	2.8	8	precision, low-noise
OP-37E	PM+	•	A	–	0.025	0.6	40	8	44	5	3.5	3.0	17[h]	63[h]	ditto, faster (decomp, min. gain = 5)
HA5147A	HA	•	–	–	0.025	0.6	40	8	44	4	3.5	3.0	35[c]	140[c]	ditto, still faster (min. gain = 10)
OP-77E	PM	•	A	A	0.025	0.3	2	6	44	2	10.3	9.6	0.3	0.6	precision
LT1028A	LT	•	–	–	0.04	0.8	90	8	44	9.5	1.0	0.85	15	75	precision ultra-low-noise
LT1013A	LT	–	•	A	0.15	2	35	4	44	1	24	22	0.4	0.8	precision single-supply
LT1055A	LT	•	–	–	0.15	4	0.05	10	40	4	28	14	13	5	precision JFET
LT1012C	LT+	•	A	–	0.05	1.5	0.15	4	40	0.6	17	14	0.2	0.8	precision low-bias
OPA111B	BB	•	A	–	0.25	1	0.001	10	36	3.5	30	7	2	2	precision low-bias JFET
AD744K	AD	•	–	–	0.5	10	0.1	9	36	4	45	18	75[f]	13[f]	ultra low dist, stable, fast settle
LTC1052	IL+	•	–	–	0.005	0.05	0.03	4.8	16	2	–	–	4	1.2	chopper
OP-90E	PM	•	A	A	0.15	2	15	1.6	36	0.02	60	60	0.012	0.02	precision micropower
CA3440A	RC	•	–	–	5	4[t]	0.04	4	15	(d)	250	110	0.003[e]	0.005[e]	nanopower (programmable)
AD549L	AD	•	–	–	0.5	10	60fA	10	36	0.7	90	35	3	1	ultra low input current JFET
LM10	NS+	•	–	–	2	2[t]	20	1.1	40	0.4	50	46	0.1	0.4	low supply voltage, rail-to-rail output

[a] see footnotes to Table 4.1. [b] • = this part number; A = available. [c] G>10. [d] programmable 0.02µA–10µA. [e] at I_s=1µA. [f] G>2. [h] G>5. [m] min/max. [t] typical.

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op-amps with the very lowest input currents (MOSFET types) generally have poor voltage offsets, and vice versa. Good circuit designers choose their components with the right trade-offs to optimize performance, without going overboard on unnecessary "gold-plated" parts.

Limitations imply trade-offs

The limitations of op-amp performance we have talked about will have an influence on component values in nearly all circuits. For instance, the feedback resistors must be large enough so that they don't load the

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"Here Yesterday, Gone Today"

In its untiring quest for better and fancier chips, the semiconductor industry can sometimes cause you great pain. It might go something like this: You've designed and prototyped a wonderful new gadget; debugging is complete, and you're ready to go into production. When you try to order the parts, you discover that a crucial IC has been discontinued by the manufacturer! An even worse nightmare goes like this: Customers have been complaining about late delivery on some instrument that you've been manufacturing for many years. When you go to the assembly area to find out what's wrong, you discover that a whole production run of boards is built, except for one IC that "hasn't come in yet." You then ask purchasing why they haven't expedited the order; turns out they have, just haven't received it. Then you learn from the distributor that the part was discontinued six months ago, and that none is available!

Why does this happen, and what do you do about it? We've generally found four reasons that ICs are discontinued:

1. *Obsolescence:* Much better parts come along, and it doesn't make much sense to keep making the old ones. This has been particularly true with digital memory chips (e.g., small static RAMs and EPROMs, which are superseded by denser and faster versions each year), though linear ICs have not entirely escaped the purge. In these cases there is often a pin-compatible improved version that you can plug into the old socket.
2. *Not selling enough:* Perfectly good ICs sometimes disappear. If you are persistent enough, you may get an explanation from the manufacturer – "there wasn't enough demand," or some such story. You might characterize this as a case of "discontinued for the convenience of the manufacturer." We've been particularly inconvenienced by Harris's discontinuation of their splendid HA4925 – a fine chip, the fastest quad comparator, now gone, with no replacement anything like it. Harris also discontinued the HA2705 – another great chip, the fastest low-power op-amp, now gone without a trace! Sometimes a good chip is discontinued when the wafer fabrication line changes over to a larger wafer size (e.g., from the original 3″ diameter wafer to a 5″ or 6″ wafer). We've noticed that Harris has a particular fondness for discontinuing excellent and unique chips; Intersil and GE have done the same thing.
3. *Lost schematics:* You might not believe it, but sometimes the semiconductor house loses track of the schematic diagram of some chip and can't make any more! This apparently happened with the Solid State Systems SSS-4404 CMOS 8-stage divider chip.
4. *Manufacturer out of business:* This also happened to the SSS-4404!

If you're stuck with a board and no available IC, you've got several choices. You can redesign the board (and perhaps the circuit) to use something that is available. This is probably best if you're going into production with a new design or if you are running a large production of an existing board. A cheap and dirty solution is to make a little "daughterboard" that plugs into the empty IC socket and includes whatever it takes to emulate the nonexistent chip. Although this latter solution isn't terribly elegant, it gets the job done.

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output significantly, but they must not be so large that input bias current produces sizable offsets. High impedances in the feedback network also increase susceptibility to capacitive pickup of interfering signals and increase the loading effects of stray capacitance. These trade-offs typically dictate resistor values of 2k to 100k with general-purpose op-amps.

Similar sorts of trade-offs are involved in almost all electronic design, including the simplest circuits constructed with transistors. For instance, the choice of quiescent current in a transistor amplifier is limited at the high end by device dissipation, increased input current, excessive supply current, and reduced current gain, whereas the lower limit of operating current is limited by leakage current, reduced current gain, and reduced speed (from stray capacitance in combination with the high resistance values). For these reasons you typically wind up with collector currents in the range of a few tens of microamps to a few tens of milliamps (higher for power circuits, sometimes a bit lower in "micropower" applications), as mentioned in Chapter 2.

In the next three chapters we will look more carefully at some of these problems in order to give you a good understanding of the trade-offs involved.

EXERCISE 4.6

Draw a dc-coupled inverting amplifier with gain of 100 and $Z_{in} = 10k$. Include compensation for input bias current, and show offset voltage trimming network (10k pot between pins 1 and 5, wiper tied to V_-). Now add circuitry so that $Z_{in} \geq 10^8$ ohms.

4.13 Low-power and programmable op-amps

For battery-powered applications there is a popular group of op-amps known as "programmable op-amps," because all of the internal operating currents are set by an externally applied current at a bias programming pin. The internal quiescent currents are all related to this bias current by current mirrors, rather than by internal resistor-programmed current sources. As a consequence, such amplifiers can be programmed to operate over a wide range of supply currents, typically from a few

POPULAR OP-AMPS

Sometimes a new op-amp comes along at just the right time, filling a vacuum with its combination of performance, convenience, and price. Several companies begin to manufacture it (it becomes "second-sourced"), designers become familiar with it, and you have a hit. Here is a list of some popular favorites of recent times:

301 First easy-to-use op-amp; first use of "lateral *pnp*." External compensation. National.

741 The industry standard for many years. Internal compensation. Fairchild.

1458 Motorola's answer to the 741; two 741s in a mini-DIP, with no offset pins.

308 National's precision op-amp. Low power, superbeta, guaranteed drift specifications.

324 Popular quad op-amp (358=dual, mini-DIP). Single-supply operation. National.

355 All-purpose bi-FET op-amp (356, 357 faster). Practically as precise as bipolar, but faster and lower input current. National. (Fairchild tried to get the FET ball rolling with their 740, which flopped because of poor performance. Would you believe 0.1V input offset?)

TL081 Texas Instruments' answer to the 355 series. Low-cost comprehensive series of singles, duals, quads; low power, low noise, many package styles.

LF411 National's improved bi-FET series. Low offset, low bias, fast, low distortion, high output current, low cost. Dual (LF412) and low-power variants (LF441/2/4).

microamps to a few milliamps. The slew rate, gain-bandwidth product f_T, and input bias current are all roughly proportional to the programmed operating current. When programmed to operate at a few microamps, programmable op-amps are extremely useful in battery-powered circuits. We will treat micropower design in detail in Chapter 14.

The 4250 was the original programmable op-amp, and it is still a good unit for many applications. Developed by Union Carbide, this classic is now "second-sourced" by many manufacturers, and it even comes in duals and triples (the 8022 and 8023, respectively). As an example of the sort of performance you can expect for operation at low supply currents, let's look at the 4250 running at 10μA. To get that operating current, we have to supply a bias current of 1.5μA with an external resistor. When it is operated at that current, f_T is 75kHz, the slew rate is 0.05V/μs, and the input bias current I_B is 3nA. At low operating currents the output drive capability is reduced considerably, and the open-loop output impedance rises to astounding levels, in this case about 3.5k. At low

THE 741 AND ITS FRIENDS

Bob Widlar designed the first really successful monolithic op-amp back in 1965, the Fairchild μA709. It achieved great popularity, but it had some problems, in particular the tendency to go into a latch-up mode when the input was overdriven and its lack of output short-circuit protection. It also required external frequency compensation (two capacitors and one resistor) and had a clumsy offset trimming circuit (again requiring three external components). Finally, its differential input voltage was limited to 5 volts.

Widlar moved from Fairchild to National, where he went on to design the LM301, an improved op-amp with short-circuit protection, freedom from latch-up, and a 30-volt differential input range. Widlar didn't provide internal frequency compensation, however, because he liked the flexibility of user compensation. The 301 could be compensated with a single capacitor, but because there was only one unused pin remaining, it still required three external components for offset trimming.

Meanwhile, over at Fairchild the answer to the 301 (the now-famous 741) was taking shape. It had the advantages of the 301, but Fairchild engineers opted for internal frequency compensation, freeing two pins to allow simplified offset trimming with a single external trimmer. Since most circuit applications don't require offset trimming (Widlar was right), the 741 in normal use requires no components other than the feedback network itself. The rest is history – the 741 caught on like wildfire and became firmly entrenched as the industry standard.

There are now numerous 741-type amps, essentially similar in design and performance, but with various features such as FET inputs, dual or quad units, versions with improved specifications, decompensated and uncompensated versions, etc. We list some of them here for reference and as a demonstration of man's instinct to clutch onto the coattails of the famous (see Table 4.1 for a more complete listing).

Single units		*Dual units*		*Quad units*	
741S	fast (10V/μs)	747	dual 741	MC4741	quad 741(alias 348)
MC741N	low noise	OP-04	precision	OP-11	precision
OP-02	precision	1458	mini-DIP package	4136	fast (3MHz)
4132	low power (35μA)	4558	fast (15V/μs)	HA4605	fast (4V/μs)
LF13741	FET low input current	TL082	FET, fast (similar to LF353)	TL084	FET, fast (similar to LF347)
748	uncompensated				
NE530	fast (25V/μs)	LF412	FET, fast		
TL081	FET, fast (similar to LF351)				
LF411	FET, fast				

the input signal; it is a full-wave rectifier. As usual, the use of op-amps and feedback eliminates the diode drops of a passive full-wave rectifier.

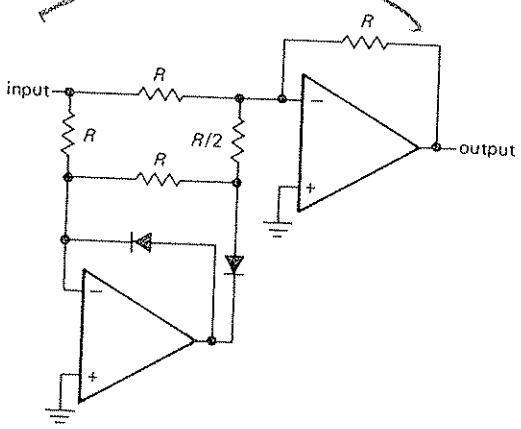


Figure 4.45. Active full-wave rectifier.

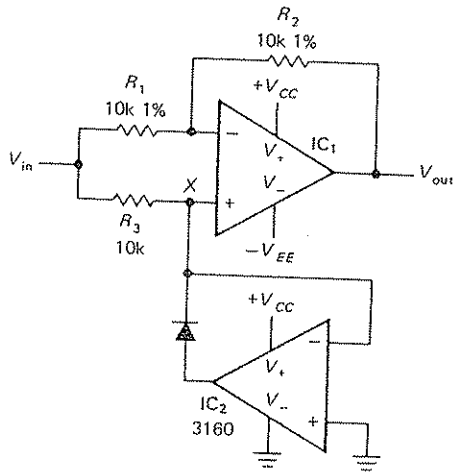


Figure 4.46

EXERCISE 4.9

Figure out how the circuit in Figure 4.45 works. Hint: Apply first a positive input voltage, and see what happens; then do negative.

Figure 4.46 shows another absolute-value circuit. It is readily understandable as a simple combination of an optional inverter (IC_1) and an active clamp (IC_2). For positive input levels the clamp is out of the circuit, with its output at negative saturation, making IC_1 a unity-gain inverter. Thus the output is equal to the absolute value of the input voltage. By running IC_2 from a single positive supply, you avoid problems of slew-rate limitations in the clamp, since its output moves over only one diode drop. Note that no great accuracy is required of R_3.

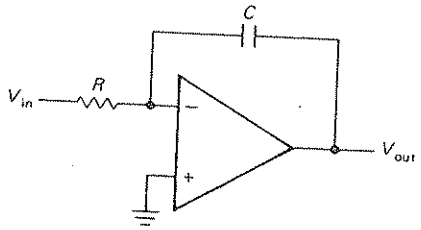


Figure 4.47. Integrator.

4.19 Integrators

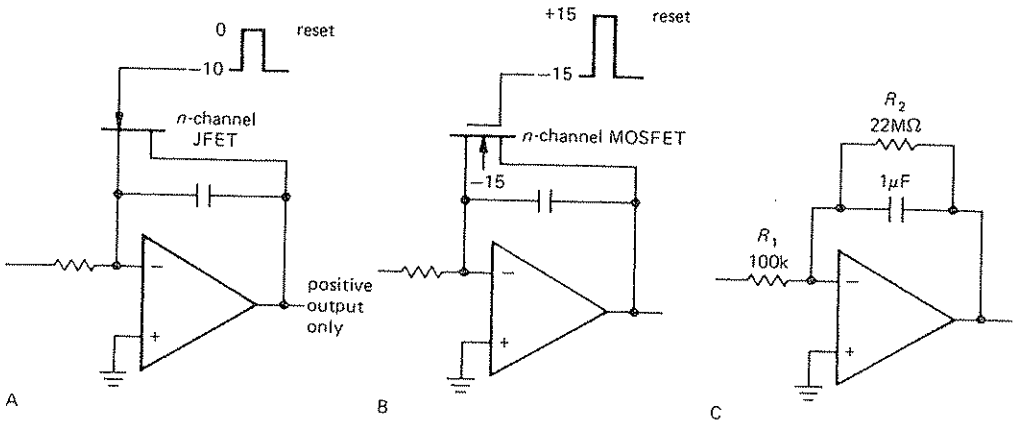
Op-amps allow you to make nearly perfect integrators, without the restriction that $V_{out} \ll V_{in}$. Figure 4.47 shows how it's done. Input current V_{in}/R flows through C. Because the inverting input is a virtual ground, the output voltage is given by

$$V_{in}/R = -C(dV_{out}/dt)$$

or

$$V_{out} = \frac{1}{RC}\int V_{in}\,dt + \text{constant}$$

The input can, of course, be a current, in which case R will be omitted. One problem with this circuit as drawn is that the output tends to wander off, even with the input grounded, due to op-amp offsets and bias current (there's no feedback at dc, which violates rule 3 in Section 4.08). This problem can be minimized by using a FET op-amp for low input current and offset, trimming the op-amp input offset voltage, and using large R and C values. In addition, in many applications the integrator is zeroed periodically by closing a



4.48. Op-amp integrators with reset switches.

switch placed across the capacitor (usually a FET), so only the drift over short time scales matters. As an example, an inexpensive FET op-amp like the LF411 (25pA typical bias current) trimmed to a voltage offset of 0.2mV and used in an integrator with $R = 10\text{M}\Omega$ and $C = 10\mu\text{F}$ will produce an output drift of less than 0.003 volt in 1000 seconds.

If the residual drift of the integrator is still too large for a given application, it may be necessary to put a large resistor R_2 across C to provide dc feedback for stable biasing. The effect is to roll off the integrator action at very low frequencies, $f < 1/R_2C$. Figure 4.48 shows integrators with FET zeroing switch and with resistor bias stabilization. The feedback resistor may become rather large in this sort of application. Figure 4.49 shows a trick for producing the effect of a large feedback resistor using smaller values. In this case the feedback network behaves like a single 10MΩ resistor in the standard inverting amplifier circuit giving a voltage gain of −100. This technique has the advantage of using resistors of convenient values without the problems of stray capacitance, etc., that occur with very large resistor values. Note that this "T-network" trick may increase the effective input offset voltage, if used in a transresistance configuration (Section 4.09). For example, the circuit of Figure 4.49, driven from a high-impedance source (e.g., the current from a photodiode, with the input resistor omitted), has an output offset of 100 times V_{os}, whereas the same circuit with a 10MΩ feedback resistor has an output equal to V_{os} (assuming the offset due to input current is negligible).

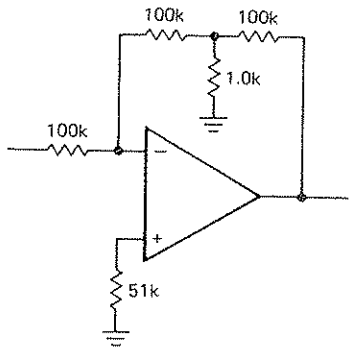


Figure 4.49

□ *A circuit cure for FET leakage*

In the integrator with a FET reset switch (Fig. 4.48), drain-source leakage sources a small current into the summing junction even when the FET is OFF. With an ultra-low-input-current op-amp and low-leakage

capacitor, this can be the dominant error in the integrator. For example, the excellent AD549 JFET-input "electrometer" op-amp has a maximum input current of 0.06pA, and a high-quality 0.01μF metallized Teflon or polystyrene capacitor specifies leakage resistance as 10^7 *meg*ohms, minimum. Thus the integrator, exclusive of reset circuit, keeps stray currents at the summing junction below 1pA (for a worst-case 10V full-scale output), corresponding to an output dV/dt of less than 0.01mV/s. Compare this with the leakage contribution of a MOSFET such as the popular 2N4351 (enhancement mode), which specifies a maximum leakage current of 10nA at $V_{DS} = 10$V and $V_{GS} = 0$V! In other words, the FET contributes 10,000 times as much leakage as everything else combined.

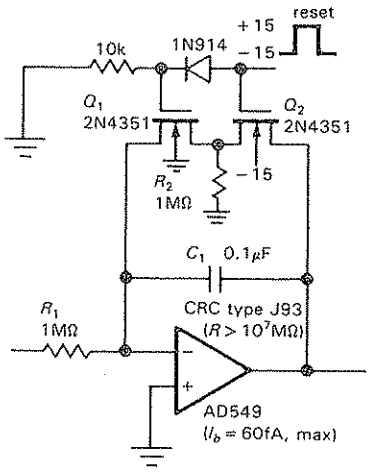


Figure 4.50

Figure 4.50 shows a clever circuit solution. Although both n-channel MOSFETs are switched together, Q_1 is switched with gate voltages of zero and +15 volts so that gate leakage (as well as drain-source leakage) is entirely eliminated during the OFF state (zero gate voltage). In the ON state the capacitor is discharged as before, but with twice R_{ON}. In the OFF state, Q_2's small leakage passes to ground through R_2 with negligible drop. There is no leakage current at the summing junction because Q_1's source, drain, and substrate are all at the same voltage. Compare this circuit with the zero-leakage peak-detector circuit of Figure 4.40.

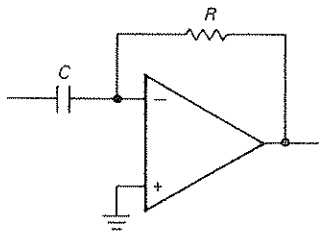


Figure 4.51

4.20 Differentiators

Differentiators are similar to integrators, but with R and C reversed (Fig. 4.51). Since the inverting input is at ground, the rate of change of input voltage produces a current $I = C(dV_{in}/dt)$ and hence an output voltage

$$V_{out} = -RC\frac{dV_{in}}{dt}$$

Differentiators are bias-stable, but they generally have problems with noise and instabilities at high frequencies because of the op-amp's high gain and internal phase shifts. For this reason it is necessary to roll off the differentiator action at some maximum frequency. The usual method is shown in Figure 4.52. The choice of the rolloff components R_1 and C_2 depends on the noise level of the signal and the bandwidth of the op-amp. At high frequencies this circuit becomes an integrator, due to R_1 and C_2.

OP-AMP OPERATION WITH A SINGLE POWER SUPPLY

Op-amps don't *require* ±15 volt regulated supplies. They can be operated from split

capable of pulling its output to ground, *even when sinking moderate current*. Some examples are the ICL76xx, the LMC660, and CA5160. (b) Op-amps with an *npn* common-emitter transistor to ground behave similarly, i.e., they can pull their output to ground even while sinking current. Examples are the LM10, CA5422, and LT1013/14. Both kinds of output stages can, of course, handle an open circuit or a load that *sinks* current to ground. (c) Some op-amps, notably the 358 and 324, use a *pnp* follower to ground (which can only pull down to within a diode drop of ground), in parallel with an *npn* current sink (with compliance clear to ground). In the 358, the internal current sink is set at 50μA. Such a circuit can swing clear down to ground as long as it doesn't have to sink more than 50μA from the load. If the load sources more current, the output only works to within a diode drop of ground. As before, this kind of output circuit is happy *sourcing* current to a load that is returned to ground (as in the photometer example earlier). (d) Finally, some single-supply op-amps (e.g., the OP-90) use a *pnp* follower to ground, without the parallel current sink. Such an output stage can swing to ground only if the load helps out by sinking current, i.e., by being returned to ground. If you want to use such an op-amp with a load that sources current, you have to add an external resistor to ground (Fig. 4.57).

A note of caution: Don't make the mistake of assuming that you can make any op-amp's output work down to the negative rail simply by providing an external current sink. In most cases the circuitry driving the output stage does not permit that. Look for explicit permission in the data sheet!

Example: single-supply dc amplifier

Figure 4.58 shows a typical single-supply noninverting amplifier to amplify an input signal of known positive polarity. The input, output, and positive supply are all referenced to ground, which is the negative supply voltage for the op-amp. The output "pulldown" resistor may be needed with what we called type-1 amplifiers to ensure output swing all the way to ground; the feedback network or the load itself could perform this function. An important point: Remember that the output cannot go negative; thus you cannot use this amplifier with, say, ac-coupled audio signals.

Single-supply op-amps are indispensable in battery-operated equipment. We'll have more to say about this in Chapter 14.

COMPARATORS AND SCHMITT TRIGGER

It is quite common to want to know which of two signals is larger, or to know when a given signal exceeds a predetermined value. For instance, the usual method of generating triangle waves is to supply positive or negative currents into a capacitor, reversing the polarity of the current when the amplitude reaches a preset peak value. Another example is a digital voltmeter. In order to convert a voltage to a number, the unknown voltage is applied to one input of a comparator, with a linear ramp (capacitor + current source) applied to the other. A digital counter counts cycles of an oscillator while the ramp is less than the unknown voltage and displays the result when equality of amplitudes is reached. The resultant count is proportional to the input voltage. This is called single-slope integration; in most sophisticated instruments a dual-slope integration is used (see Section 9.21).

4.23 Comparators

The simplest form of comparator is a high-gain differential amplifier, made either with transistors or with an op-amp (Fig. 4.59). The op-amp goes into positive or

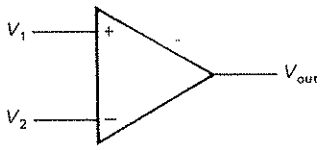


Figure 4.59

negative saturation according to the difference of the input voltages. Because the voltage gain typically exceeds 100,000, the inputs will have to be equal to within a fraction of a millivolt in order for the output not to be saturated. Although an ordinary op-amp can be used as a comparator (and frequently is), there are special integrated circuits intended for use as comparators. Some examples are the LM306, LM311, LM393, NE527, and TLC372. These chips are designed for very fast response and aren't even in the same league as op-amps. For example, the high-speed NE521 slews at several thousand volts per microsecond. With comparators, the term "slew rate" isn't usually used; you talk instead about "propagation delay versus input overdrive."

Comparators generally have more flexible output circuits than op-amps. Whereas an ordinary op-amp uses a push-pull output stage to swing between the supply voltages (±13V, say, for a 411 running from ±15V supplies), a comparator chip usually has an "open-collector" output with grounded emitter. By supplying an external "pullup" resistor (that's accepted terminology, believe it or not) connected to a voltage of your choice, you can have an output swing from +5 volts to ground, say. You will see later that logic circuits have well-defined voltages they like to operate between; the preceding example would be ideal for driving a TTL circuit, a popular type of digital logic. Figure 4.60 shows the circuit. The output switches from +5 volts to ground when the input signal goes negative. This use of a comparator is really an example of analog-to-digital conversion.

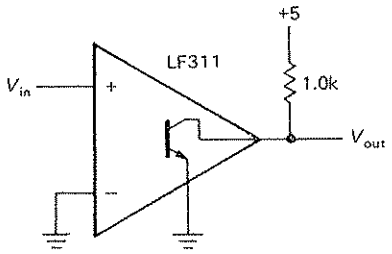


Figure 4.60

This is the first example we have presented of an *open-collector* output; this is a common configuration in logic circuits, as you will see throughout Chapters 8–11. If you like, you can think of the external pullup resistor as completing the comparator's internal circuit by providing a collector load resistor for an *npn* output transistor. Since the output transistor operates as a saturated switch, the resistor value is not at all critical, with values typically between a few hundred ohms and a few thousand ohms; small values yield improved switching speed and noise immunity at the expense of increased power dissipation. Incidentally, in spite of their superficial resemblance to op-amps, comparators are never used with negative feedback because they would not be stable (see Sections 4.32–4.34). However, some *positive* feedback is often used, as you will see in the next section.

Comments on comparators

Some points to remember: (a) Because there is no negative feedback, golden rule I is not obeyed. The inputs are not at the same voltage. (b) The absence of negative feedback means that the (differential) input impedance isn't bootstrapped to the high values characteristic of op-amp circuits. As a result, the input signal sees a changing load and changing (small) input current as the comparator switches; if the driving impedance is too high,

strange things may happen. (c) Some comparators permit only limited differential input swings, as little as ±5 volts in some cases. Check the specs! See Table 9.3 and the discussion in Section 9.07 for the properties of some popular comparators.

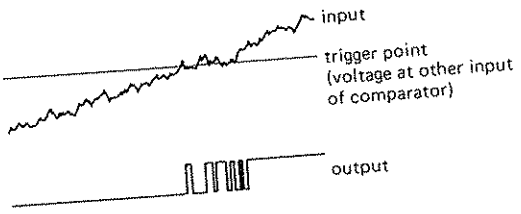
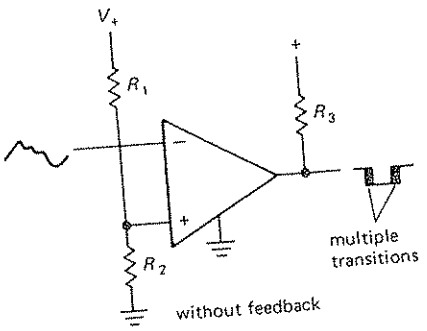


Figure 4.61



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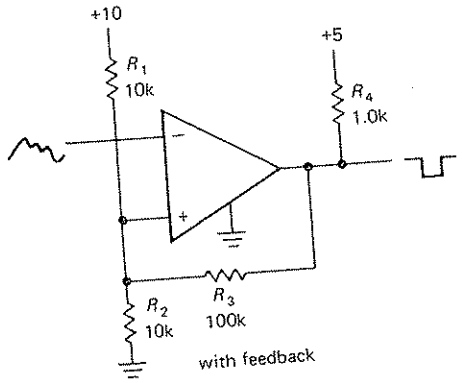

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Figure 4.62

4.24 Schmitt trigger

The simple comparator circuit in Figure 4.60 has two disadvantages. For a very slowly varying input, the output swing can be rather slow. Worse still, if the input is noisy, the output may make several transitions as the input passes through the trigger point (Fig. 4.61). Both these problems can be remedied by the use of *positive* feedback (Fig. 4.62). The effect of R_3 is to make the circuit have two thresholds, depending on the output state. In the example shown, the threshold when the output is at ground (input high) is 4.76 volts, whereas the threshold with the output at +5 volts is 5.0 volts. A noisy input is less likely to produce multiple triggering (Fig. 4.63). Furthermore, the positive feedback ensures a rapid output transition, regardless of the speed of the input waveform. (A small "speedup" capacitor of 10–100pF is often connected across R_3 to enhance switching speed still further.) This configuration is known as a Schmitt trigger. (If an op-amp were used, the pullup would be omitted.)

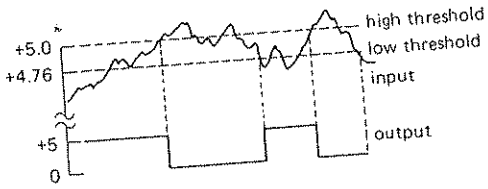

Figure 4.63

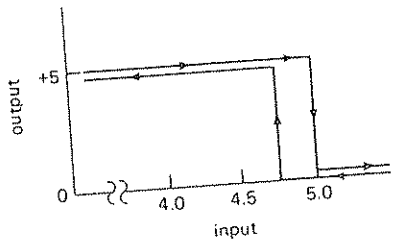

Figure 4.64

The output depends both on the input voltage and on its recent history, an effect called *hysteresis*. This can be illustrated with a diagram of output versus input, as in Figure 4.64. The design procedure

is easy for Schmitt triggers that have a small amount of hysteresis. Use the circuit of Figure 4.62B. First choose a resistive divider (R_1, R_2) to put the threshold at approximately the right voltage; if you want the threshold near ground, just use a single resistor from noninverting input to ground. Next, choose the (positive) feedback resistor R_3 to produce the required hysteresis, noting that the hysteresis equals the output swing, attenuated by a resistive divider formed by R_3 and $R_1 \| R_2$. Finally, choose an output pullup resistor R_4 small enough to ensure nearly full supply swing, taking account of the loading by R_3. For the case where you want thresholds symmetrical about ground, connect an offsetting resistor of appropriate value from the noninverting input to the negative supply. You may wish to scale all resistor values in order to keep the output current and impedance levels within a reasonable range.

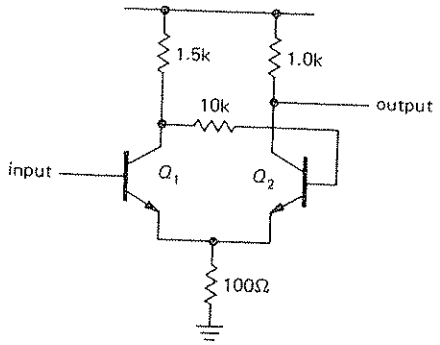

Figure 4.65

Discrete-transistor Schmitt trigger

A Schmitt trigger can also be made simply with transistors (Fig. 4.65). Q_1 and Q_2 share an emitter resistor. It is essential that Q_1's collector resistor be larger than Q_2's. In that way the threshold to turn on Q_1, which is one diode drop above the emitter voltage, rises when Q_1 is turned off, since the emitter current is higher with Q_2 conducting. This produces hysteresis in the trigger threshold, just as in the preceding integrated circuit Schmitt trigger.

EXERCISE 4.10

Design a Schmitt trigger using a 311 comparator (open-collector output) with thresholds at +1.0 volt and +1.5 volts. Use a 1.0k pullup resistor to +5 volts, and assume that the 311 is powered from ±15 volt supplies.

FEEDBACK WITH FINITE-GAIN AMPLIFIERS

We mentioned in Section 4.12 that the finite open-loop gain of an op-amp limits its performance in a feedback circuit. Specifically, the closed-loop gain can never exceed the open-loop gain, and as the open-loop gain approaches the closed-loop gain, the amplifier begins to depart from the ideal behavior we have come to expect. In this section we will quantify these statements so that you will be able to predict the performance of a feedback amplifier constructed with real (less than ideal) components. This is important also for feedback amplifiers constructed entirely with discrete components (transistors), where the open-loop gain is usually much less than with op-amps. In these cases the output impedance, for instance, will not be zero. Nonetheless, with a good understanding of feedback principles you will be able to achieve the performance required in any given circuit.

4.25 Gain equation

Let's begin by considering an amplifier of finite voltage gain, connected with feedback to form a noninverting amplifier (Fig. 4.66). The amplifier has open-loop voltage gain A, and the feedback network subtracts a fraction B of the output voltage from the input. (Later we will generalize

things so that inputs and outputs can be currents or voltages.) The input to the gain block is then $V_{in} - BV_{out}$. But the output is just the input times A:

$$A(V_{in} - BV_{out}) = V_{out}$$

In other words,

$$V_{out} = \frac{A}{1 + AB} V_{in}$$

and the closed-loop voltage gain, V_{out}/V_{in}, is just

$$G = \frac{A}{1 + AB}$$

Some terminology: The standard designations for these quantities are as follows: G = closed-loop gain, A = open-loop gain, AB = loop gain, $1 + AB$ = return difference, or desensitivity. The feedback network is sometimes called the beta network (no relation to transistor beta, h_{fe}).

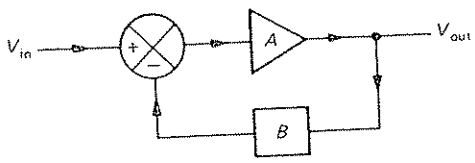

Figure 4.66

4.26 Effects of feedback on amplifier circuits

Let's look at the important effects of feedback. The most significant are predictability of gain (and reduction of distortion), changed input impedance, and changed output impedance.

Predictability of gain

The voltage gain is $A/(1 + AB)$. In the limit of infinite open-loop gain A, $G = 1/B$. We saw this result in the noninverting amplifier configuration, where a voltage divider on the output provided the signal to the inverting input (Fig. 4.69). The closed-loop voltage gain was just the inverse of the division ratio of the voltage divider. For finite gain A, feedback still acts to reduce the effects of variations of A (with frequency, temperature, amplitude, etc.). For instance, suppose A depends on frequency as in Figure 4.67. This

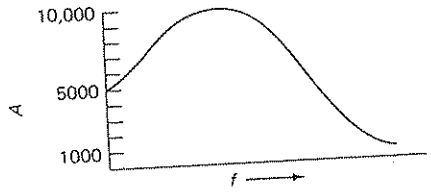

Figure 4.67

will surely satisfy anyone's definition of a poor amplifier (the gain varies over a factor of 10 with frequency). Now imagine we introduce feedback, with $B = 0.1$ (a simple voltage divider will do). The closed-loop voltage gain now varies from 1000/[1 +(1000×0.1)], or 9.90, to 10,000/[1 + (10,000×0.1)], or 9.99, a variation of just 1% over the same range of frequency! To put it in audio terms, the original amplifier is flat to ±10dB, whereas the feedback amplifier is flat to ±0.04dB. We can now recover the original gain of 1000 with nearly this linearity by just cascading three such stages. It was for just this reason (namely, the need for extremely flat telephone repeater amplifiers) that negative feedback was invented. As the inventor, Harold Black, described it in his first open publication on the invention (*Electrical Engineering*, 53:114, 1934), "by building an amplifier whose gain is made deliberately, say 40 decibels higher than necessary (10,000-fold excess on energy basis) and then feeding the output back to the input in such a way as to throw away the excess gain, it has been found possible to effect extraordinary improvement in constancy of amplification and freedom from nonlinearity."

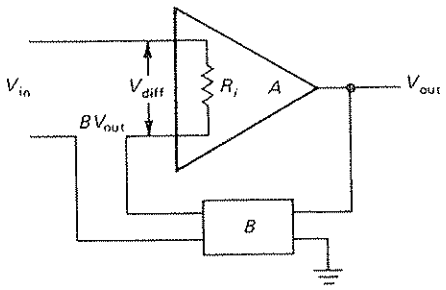

Figure 4.68

It is easy to show, by taking the partial derivative of G with respect to A ($\partial G/\partial A$), that relative variations in the open-loop gain are reduced by the desensitivity:

$$\frac{\Delta G}{G} = \frac{1}{1+AB}\frac{\Delta A}{A}$$

Thus, for good performance the loop gain AB should be much larger than 1. That's equivalent to saying that the open-loop gain should be much larger than the closed-loop gain.

A very important consequence of this is that nonlinearities, which are simply gain variations that depend on signal level, are reduced in exactly the same way.

Input impedance

Feedback can be arranged to subtract a voltage or a current from the input (these are sometimes called *series feedback* and *shunt feedback*, respectively). The noninverting op-amp configuration, for instance, subtracts a sample of the output voltage from the differential voltage appearing at the input, whereas in the inverting configuration a current is subtracted from the input. The effects on input impedance are opposite in the two cases: Voltage feedback multiplies the open-loop input impedance by $1 + AB$, whereas current feedback reduces it by the same factor. In the limit of infinite loop gain the input impedance (at the amplifier's input terminal) goes to infinity or zero, respectively. This is easy to understand, since voltage feedback tends to subtract signal from the input, resulting in a smaller change (by the factor AB) across the amplifier's input resistance; it's a form of bootstrapping. Current feedback reduces the input signal by bucking it with an equal current.

Let's see explicitly how the effective input impedance is changed by feedback. We will illustrate the case of voltage feedback only, since the derivations are similar for the two cases. We begin with an op-amp model with (finite) input resistance as shown in Figure 4.68. An input V_{in} is reduced by BV_{out}, putting a voltage $V_{diff} = V_{in} - BV_{out}$ across the inputs of the amplifier. The input current is therefore

$$I_{in} = \frac{V_{in} - BV_{out}}{R_i} = \frac{V_{in}\left(1 - B\frac{A}{1+AB}\right)}{R_i} = \frac{V_{in}}{(1+AB)R_i}$$

giving an effective input resistance

$$R_i' = V_{in}/I_{in} = (1+AB)R_i$$

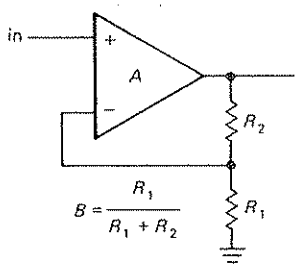

Figure 4.69

The classic op-amp noninverting amplifier is exactly this feedback configuration, as shown in Figure 4.69. In this circuit, $B = R_1/(R_1 + R_2)$, giving the usual voltage-gain expression $G_v = 1 + R_2/R_1$ and an infinite input impedance for the ideal case of infinite open-loop voltage gain

A. For finite loop gain, the equations as previously derived apply.

The op-amp *inverting* amplifier circuit is different from the noninverting circuit and has to be analyzed separately. It's best to think of it as a combination of an input resistor driving a shunt feedback stage (Fig. 4.70). The shunt stage alone has its input at the "summing junction" (the inverting input of the amplifier), where the currents from feedback and input signals are combined (this amplifier connection is really a "transresistance" configuration; it converts a current input to a voltage output). Feedback reduces the impedance looking into the summing junction, R_2, by a factor of $1 + A$ (see if you can prove this). In cases of very high loop gain (e.g, an op-amp) the input impedance is reduced to a fraction of an ohm, a good characteristic for a current-input amplifier. Some good examples are the photometer amplifier in Section 4.22 and the logarithmic converter in Section 4.14.

The classic op-amp inverting amplifier connection is a combination of a shunt feedback transresistance amplifier and a series input resistor, as in the figure. As a result, the input impedance equals the sum of R_1 and the impedance looking into the summing junction. For high loop gain, R_{in} approximately equals R_1.

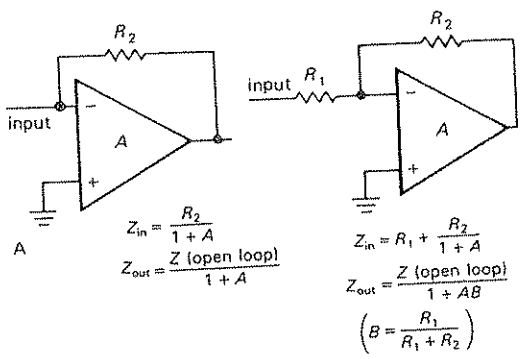

Figure 4.70. Input and output impedances for (A) transresistance amplifier and (B) inverting amplifier.

It is a straightforward exercise to derive an expression for the closed-loop voltage gain of the inverting amplifier with finite loop gain. The answer is

$$G = -A(1 - B)/(1 + AB)$$

where B is defined as before, $B = R_1/(R_1 + R_2)$. In the limit of large open-loop gain A, $G = -1/B + 1$ (i.e., $G = -R_2/R_1$).

EXERCISE 4.11

Derive the foregoing expressions for input impedance and gain of the inverting amplifier.

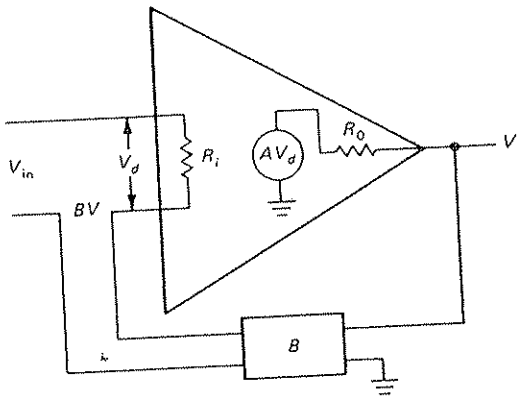

Figure 4.71

Output impedance

Again, feedback can extract a sample of the output voltage or the output current. In the first case the open-loop output impedance will be reduced by the factor $1 + AB$, whereas in the second case it will be increased by the same factor. We will illustrate this effect for the case of voltage sampling. We begin with the model shown in Figure 4.71. This time we have shown the output impedance explicitly. The calculation is simplified by a trick: Short the input, and apply a voltage V to the output; by calculating the output current I, we get the output impedance $R_0' = V/I$. Voltage V at the output

puts a voltage $-BV$ across the amplifier's input, producing a voltage $-ABV$ in the amplifier's internal generator. The output current is therefore

$$I = \frac{V-(-ABV)}{R_0} = \frac{V(1+AB)}{R_0}$$

giving an effective output impedance

$$R_0' = V/I = R_0/(1+AB)$$

If feedback is connected instead to sample the output current, the expression becomes

$$R_0' = R_0(1+AB)$$

It is possible to have multiple feedback paths, sampling both voltage and current. In the general case the output impedance is given by Blackman's impedance relation

$$R_0' = R_0\frac{1+(AB)_{SC}}{1+(AB)_{OC}}$$

where $(AB)_{SC}$ is the loop gain with the output shorted to ground and $(AB)_{OC}$ is the loop gain with no load attached. Thus, feedback can be used to generate a desired output impedance. This equation reduces to the previous results for the usual situation in which feedback is derived from either the output voltage or the output current.

☐ *Loading by the feedback network*

In feedback computations, you usually assume that the beta network doesn't load the amplifier's output. If it does, that must be taken into account in computing the open-loop gain. Likewise, if the connection of the beta network at the amplifier's input affects the open-loop gain (feedback removed, but network still connected), you must use the modified open-loop gain. Finally, the preceding expressions assume that the beta network is unidirectional, i.e., it does not couple signal from the input to the output.

☐ 4.27 Two examples of transistor amplifiers with feedback

Figure 4.72 shows a transistor amplifier with negative feedback.

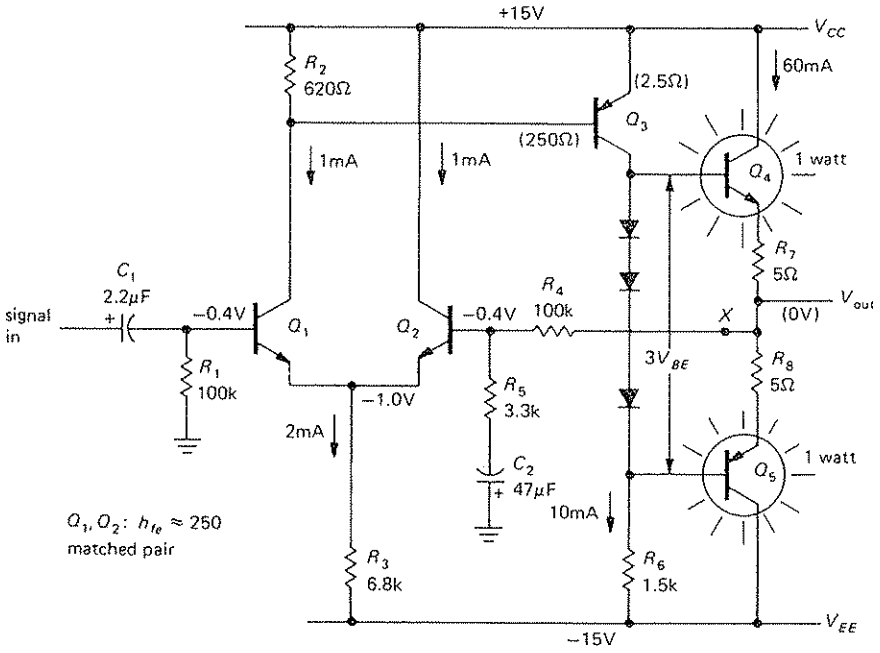

Figure 4.72. Transistor power amplifier with negative feedback.

gain at the quiescent point is 3.5 × 600, or 2100. Since Q_3's gain depends on its collector current, there is substantial change of gain with signal swing, i.e., nonlinearity. The gain is tabulated in the following section for three values of output voltage.

☐ *Closed loop.* Input impedance: This circuit uses series feedback, so the input impedance is raised by (1 + loop gain). The feedback network is a voltage divider with $B = 1/30$ at signal frequencies, so the loop gain AB is 70. The input impedance is therefore 70 × 16k, still paralleled by the 100k bias resistor, i.e., about 92k. The bias resistor now dominates the input impedance.

Output impedance: Since the output *voltage* is sampled, the output impedance is reduced by (1 + loop gain). The output impedance is therefore 0.3 ohm. Note that this is a small-signal impedance and does not mean that a 1 ohm load could be driven to nearly full swing, for instance. The 5 ohm emitter resistors in the output stage limit the large signal swing. For instance, a 4 ohm load could be driven only to 10 volts pp, approximately.

Gain: The gain is $A/(1+AB)$. At the quiescent point, that equals 30.84, using the exact value for B. In order to illustrate the gain stability achieved with negative feedback, the overall voltage gain of the circuit with and without feedback is tabulated at three values of output level at the end of this paragraph. It should be obvious that negative feedback has brought about considerable improvement in the amplifier's characteristics, although in fairness it should be pointed out that the amplifier could have been designed for better open-loop performance, e.g., by using a current source for Q_3's collector load and degenerating its emitter, by using a current source for the differential-pair emitter circuit, etc. Even so, feedback would still make a large improvement.

	Open loop			*Closed loop*		
V_{out}	−10	0	+10	−10	0	+10
Z_{in}	16k	16k	16k	92k	92k	92k
Z_{out}	20Ω	20Ω	20Ω	0.3Ω	0.3Ω	0.3Ω
Gain	1360	2100	2400	30.60	30.84	30.90

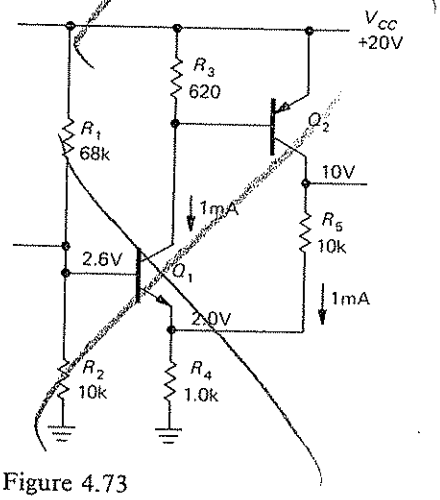

Figure 4.73

☐ ***Series feedback pair***

Figure 4.73 shows another transistor amplifier with feedback. Thinking of Q_1 as an amplifier of its base-emitter voltage drop (thinking in the Ebers-Moll sense), the feedback samples the output voltage and subtracts a fraction of it from the input signal. This circuit is a bit tricky because Q_2's collector resistor doubles as the feedback network. Applying the techniques we used earlier, you should be able to show that G(open loop) ≈ 200, loop gain ≈ 20, Z_{out}(open loop) ≈10k, Z_{out}(closed loop) ≈ 500 ohms, and G(closed loop) ≈ 9.5.

SOME TYPICAL OP-AMP CIRCUITS

4.28 General-purpose lab amplifier

Figure 4.74 shows a dc-coupled "decade amplifier" with settable gain, bandwidth, and wide-range dc output offset. IC_1 is a FET-input op-amp with noninverting gain from unity (0dB) to ×100 (40dB) in

accurately calibrated 10dB steps; a vernier is provided for variable gain. IC_2 is an inverting amplifier; it allows offsetting the output over a range of ±10 volts, accurately calibrated via R_{14}, by injecting current into the summing junction. $C_2 - C_4$ set the high-frequency rolloff, since it is often a nuisance to have excessive bandwidth (and noise). IC_5 is a power booster for driving low-impedance loads or cables; it can provide ±150mA output current.

Some interesting details: A 10MΩ input resistor is small enough, since the bias current of the 411 is 25pA (0.3mV error with open input). R_2, in combination with D_1 and D_2, limits the input voltage at the op-amp to the range V_- to $V_+ + 0.7$. D_3 is used to generate a clamp voltage at $V_- + 0.7$, since the input common mode range extends only to V_- (exceeding V_- causes the output to reverse phase). With the protection components shown, the input can go to ±150 volts without damage.

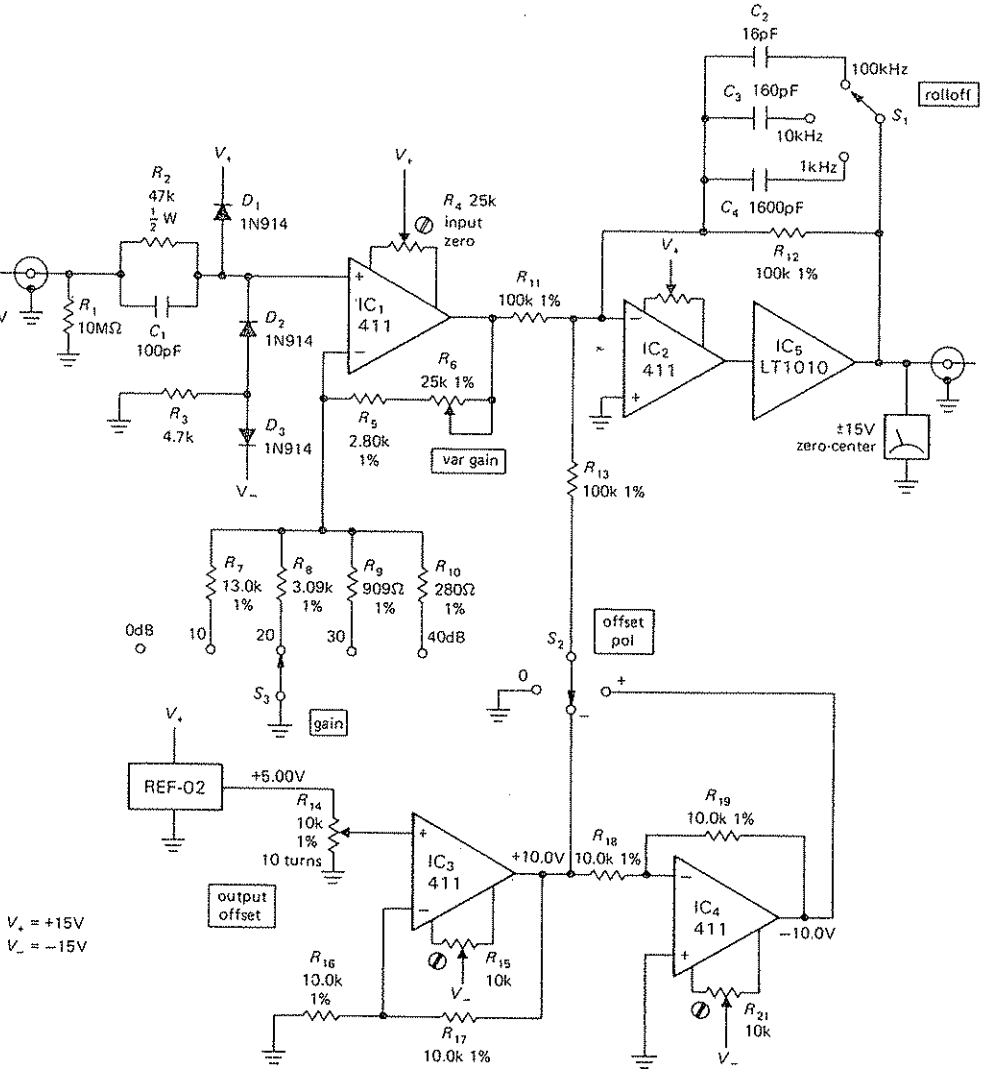

Figure 4.74. Laboratory dc amplifier with output offset.