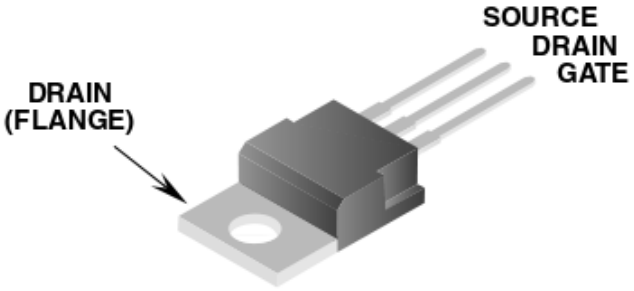
Physics 364, Fall 2012, Lab #7

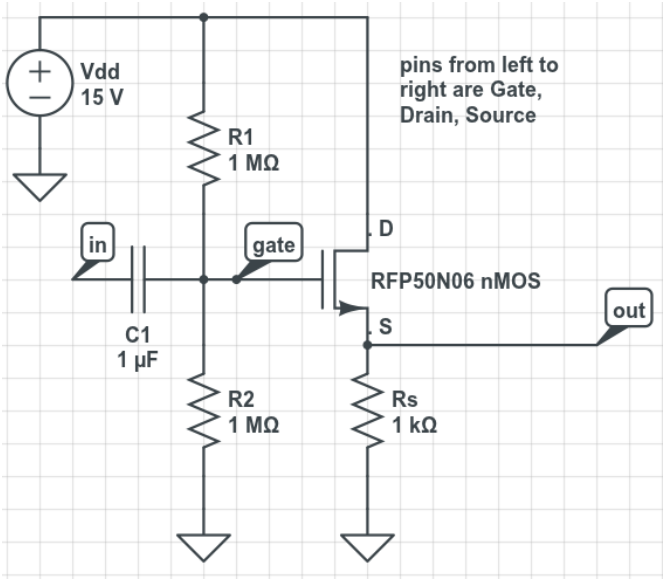
(Transistors III: field-effect transistors)

start Wednesday, October 24 — finish Monday, October 29.

Course materials and schedule are at `positron.hep.upenn.edu/p364`

Lab #7 is the last of three transistor labs. This week, we look at Field Effect Transistors. After seeing that FETs can be used in many of the same circuits that we are used to building with BJTs, you will try out the DG403 analog switch, which is a FET-based ON/OFF switch that is controlled by a circuit signal rather than by your fingers. Finally, we will revisit the home-made opamp concept.





Part 1: nMOS source follower

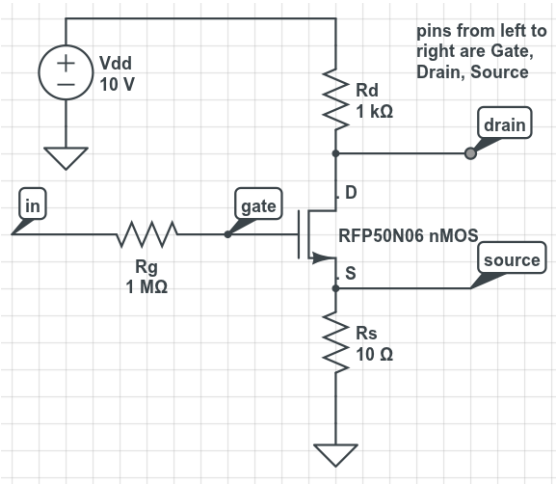
Build the nMOS source follower shown above, using $V_{DD} = +15$ V. A source follower is the FET equivalent of an emitter follower. (Remember that emitter, base, and collector are analogous to source, gate, and drain. Also remember that an n-channel MOSFET (a.k.a. nMOS) is the MOSFET analogue of an NPN bipolar transistor.) Convince yourself that the FET's input resistance is very large. (For example, you might do this by putting a very large resistor in series with the gate (between the biasing network and the gate) and noticing that there is no detectable voltage drop across it.) By comparing V_{gate} with V_{source}, see if you can figure out what $V_{\text{threshold}}$ is for this FET: that's the value of V_{GS} at which I_D becomes non-negligible.

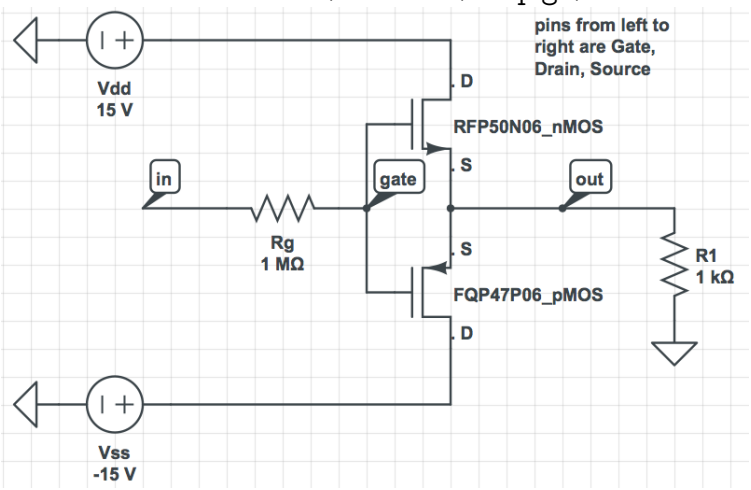
In the next part of the lab, we'll measure some of the characteristics of this MOSFET. You're seeing it work first as a follower so that you can be sure that you're measuring a working FET and that you know which pins are which.

If you're feeling lazy, you can study and modify this circuit online at `www.circuitlab.com/circuit/2ede5v` .

Part 2: n-channel MOSFET characteristics

Build the circuit shown below (left), which will allow you to measure the turn-on curve of I_{DS} vs. V_{GS} by analogy with the measurements that you made in Lab 5 of an NPN transistor. Use $V_{DD} = +10$ V (though you can try other values, if you like, to vary V_{DS}), and drive V_{in} from either your +6 V power supply or your function generator at a very low frequency. Measure V_{gate}, V_{source}, and V_{drain} as you vary V_{in}, and then estimate I_D vs. V_{GS}. Does the curve look quadratic? What is $V_{\text{threshold}}$? What is the constant K for this MOSFET (in units of A/V^2)? Do you see any evidence of gate current? Remember that $I_D = K \cdot (V_{GS} - V_t)^2$ in active mode. This quadratic rise is in sharp contrast with the exponential rise of I_C vs. V_{BE} for a bipolar transistor. Also, the data sheet lists a wide range for $V_{\text{threshold}}$: anywhere from 2 V to 4 V. This large part-by-part variation is typical of FETs. If you're feeling extremely lazy, you can measure this online circuit instead: `www.circuitlab.com/circuit/v5qcgc/` .



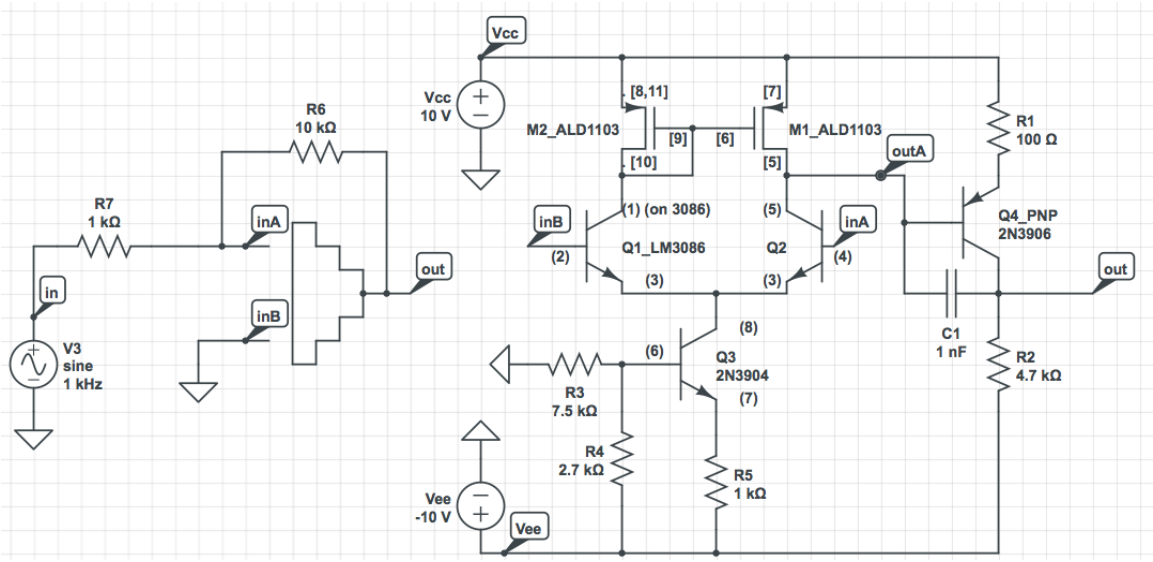


Part 3: CMOS push-pull follower

Build the CMOS (complementary MOS) push-pull follower shown above (right), using one nMOS and one pMOS FET. The pins go Gate, Drain, Source from left to right for both the nMOS (RFP50N06) and the pMOS (FQP47P06) FETs. Use $V_{DD} = +15$ V and $V_{SS} = -15$ V. Drive V_{in} with a sine wave about 8 V in amplitude. Because of the large $V_{\text{threshold}}$, the crossover distortion will be quite noticeable. Looking for a voltage drop across the 1 MΩ resistor, do you see any sign of nonzero gate current? (If the frequency of your input signal is too large, it is possible that you may see evidence of the FET's capacitance.) **Try to reach this point by the end of the first day.** If you are running short on time, look at the online version of this circuit at `www.circuitlab.com/circuit/kwy7z3/` .

Part 4: DG403 analog switch experiments

Please see the attached handout from the Harvard course, which will lead you through several exercises with the DG403 analog switch (whose internal workings use MOSFETs as ON/OFF switches). It should take you just over two hours to go through those lab exercises. It's no problem if it stretches out into part of the third day.



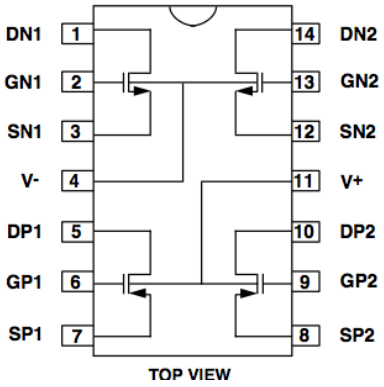
Part 5: home-made opamp revisited

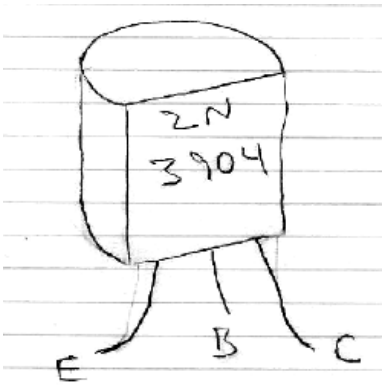
The figure above shows the home-made opamp (version 2.0) that I described in this week's notes. It has the same general form as the circuit we studied in class at the end of last week, but the output stage has been omitted for simplicity. So we have just a high-gain differential amplifier (using two matched NPN transistors) followed by a second stage which is a PNP-based common-emitter amplifier. In real life, we would add a follower as a third stage to reduce the output resistance, but I want to keep the parts count small enough to give you some chance of actually building the circuit, if you so choose.

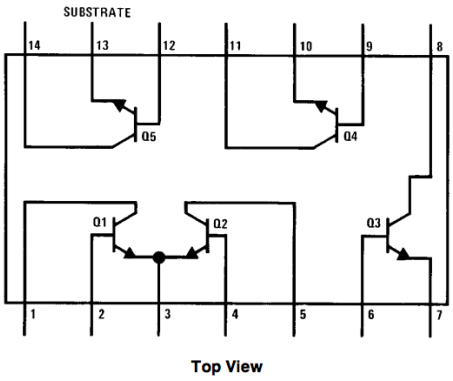
If you don't feel ambitious enough to try to build the circuit in real hardware, just study the online model at `www.circuitlab.com/circuit/fuh3fz/` .

If you do want to build this circuit in real hardware, you need to use two matched NPN transistors from an LM3086 transistor array for Q_1 and Q_2, and you need to use two matched pMOS transistors from an ALD1103 MOSFET array for M_1 and M_2. Use $+10$ V and -10 V for the power supply voltages (as this MOSFET array is only rated for 10.6 V between drain and source). Be very careful about static electricity when handling the MOSFET array, as the gate electrode can easily be destroyed. On the ALD1103 one pMOS transistor uses pins 7=source, 6=gate, 5=drain; and the other pMOS transistor uses pins 8=source, 9=gate, 10=drain. Connect the two sources (pins 7 and 8) to +10 V; also connect the pMOS substrate (pin 11) to +10 V. The schematic diagram shows in square brackets [] the ALD1103 pin numbers and in round parentheses () the LM3086 pin numbers. You might as well also use the LM3086 array for Q_3, though it has no need to be matched to the others. Unfortunately, you need a separate 2N3906 PNP transistor for Q_4, since the transistor array contains only NPN transistors. Also notice that the emitters of Q_1 and Q_2 are internally wired together: the reason why is that this differential pair configuration is a common use of transistor arrays.

What else can you do to test whether the circuit works as an opamp? Can you easily see its imperfections, e.g. V_{offset}? Can you see how the opamp's gain decreases with frequency? If you make the 1 nF compensation capacitor larger, how does this affect the frequency dependence of the opamp's gain? Can you measure (or put some sort of bound on) the gain of the first and second stages of this opamp? (This is easy to do in the simulation, but probably pretty tricky to do in the real hardware.)







The left figure above shows the pin assignments for the ALD1103 MOSFET array. You want to use transistors "P_1" and "P_2" (pins 5–11). Note that the pMOS transistors appear upside-down: the source will appear above the drain for pMOS on your schematic diagram.

The middle figure above shows the 2N3904 pinout, which also works for the PNP 2N3906 transistor. You want a 3906 (PNP), not a 3904 (NPN).

The right figure above shows the pin assignments for the LM3086 NPN transistor array. You'll use transistors Q_1 and Q_2 for the differential pair, and Q_3 for the current source that sits in the "tail" of the differential pair.