

# Physics 364, Fall 2012, Lab #8

*(Digital logic introduction)*

start Wednesday, October 31 — finish Friday, November 2.

Course materials and schedule are at [positron.hep.upenn.edu/p364](http://positron.hep.upenn.edu/p364)

Lab #8 is a very brief introduction to the digital world of ones and zeros. We will study logic gates in more detail just after Thanksgiving, when we work with Field Programmable Gate Arrays (FPGAs, a.k.a. programmable logic). Because we lost a day to Hurricane Sandy, this lab will be relatively brief and informal. Next Monday we will start working with Arduino processors, so that you get some feeling for what a small computer can do. Then in the last part of the course we will try to look under the hood to gain some intuition about how a simplified computer can be built up from logic gates.

## Part 1

For the first part of the lab, please find file

[http://positron.hep.upenn.edu/wja/P364\\_2012/ese111\\_lab2.pdf](http://positron.hep.upenn.edu/wja/P364_2012/ese111_lab2.pdf)

and work your way through parts 1 through 5 of that lab, which is borrowed from UPenn course ESE111. If you find any part of this lab insufferably boring, just write down in your lab notebook enough to demonstrate that you understand the idea and point out that going through the exercise step-by-step would ruin your day. Then again, I think you might find parts of these exercises to be quite fun.

## Part 2

Go over to [circuitlab.com](http://circuitlab.com) and study at least a couple of the following circuits. Make sure that you can trace your way through the pieces of the inverter and the NAND gate to understand how the collection of nMOS and pMOS FETs manages to carry out the NOT (inverter) and the NAND functions. This means looking at  $V_{GS}$  for each FET for each of the two possible input states of the inverter circuit and for each of the four possible input states of the NAND circuit. Be sure to consider the difference between the  $n$ -channel and  $p$ -channel MOSFETs. If you have time, then also study the AND circuit and the NOR circuit.

[circuitlab.com/circuit/rh9apy/cmos-inverter-phys-364-lab-8-part-1/](http://circuitlab.com/circuit/rh9apy/cmos-inverter-phys-364-lab-8-part-1/)

[circuitlab.com/circuit/vv5j73/cmos-buffer-phys-364-lab-8/](http://circuitlab.com/circuit/vv5j73/cmos-buffer-phys-364-lab-8/)

[circuitlab.com/circuit/xewn6p/cmos-nand-gate/](http://circuitlab.com/circuit/xewn6p/cmos-nand-gate/)

[circuitlab.com/circuit/rw75pc/cmos-and-gate/](http://circuitlab.com/circuit/rw75pc/cmos-and-gate/)

[circuitlab.com/circuit/w595t9/cmos-nor-gate/](http://circuitlab.com/circuit/w595t9/cmos-nor-gate/)