9.8/10

Lab #8 - Intro Digital Logic

Phys 364 - Measurements Lab (Bill & Jose)

Part 1

a) TTL inverter: The schematic roughly makes sense. When there's 0V of input voltage, the +5V source supplies voltage such that Y is also ~+5V, and when there's +5V input, the base of Q3 has a positive voltage applied (~.6V according to SPICE), and there's a connection between Y and ground which produces the OFF state.

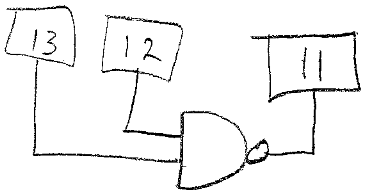
b) the truth table for NAND is →

A	B	Y
0	0	high
0	1	high
1	0	high
1	1	low

and we can see that on the SPICE output, Y drops to low when the out-of-phase square waves are both on. The maximum drain of current at the output occurs when the circuit switches to the high state, at which time the maximum current is about 37mA. The symmetric low-state spikes are smaller.

PART 2

a) - Using a TI SN74LS00N NAND gate instead of the 74LS04 TTL inverter and grounding one input produces the same results.

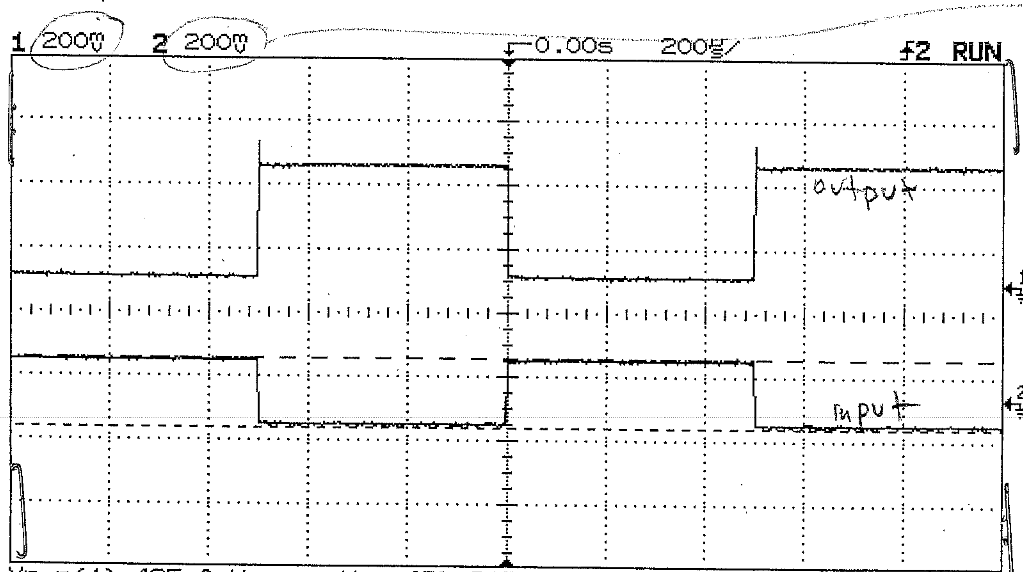


12 is tied to +5V

13	12	NAND out
0	0	1
1	0	0

=> inversion!

- confirmed experimentally - the output waveform is the inverse of the input:



Should adjust oscilloscope for 10X pr

(after adding a DC offset, signals were cleaner.)

V_{in}	V_{out} (V)
.440	.4
.470	.42
.53	.44
.62	.45
.675	.46

↙ V_{out} remains at about .46 V on the upper end of the input.

The specs supply the maximum output current as $-0.4\,mA \le I \le 8.0\,mA$, and 0 to ~.35 $\le V_{Low} \le .5$, so V_{low} is reasonable.

b) The LED connected to the +5 is far brighter than the LED connected between V_{out} and gnd — the currents are 23mA and 5mA for each respective state.

c) My inverter correctly drove the LEDs after I remembered the resistors that bring the output down to ground in the OFF state.

PART 3

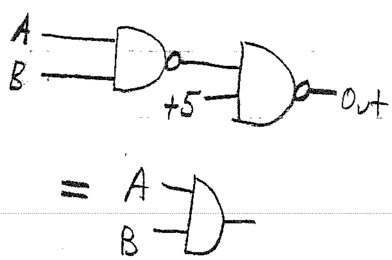
NAND

a)

A	B	Out
0	0	1
0	1	1
1	0	1
1	1	0

– the chip outputs correctly.

b)



want AND

A	B	Out
0	0	0
0	1	0
1	0	0
1	1	1

– output confirmed.

c) The AND truth table was confirmed yet again.

d) OR

A	B	Out
0	0	0
0	1	1
1	0	1
1	1	1

– confirmed.

e) XOR

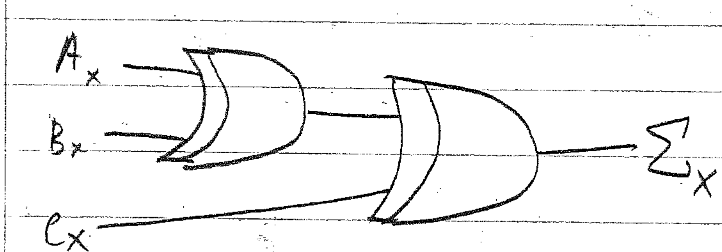
A	B	Out
0	0	0
0	1	1
1	0	1
1	1	0

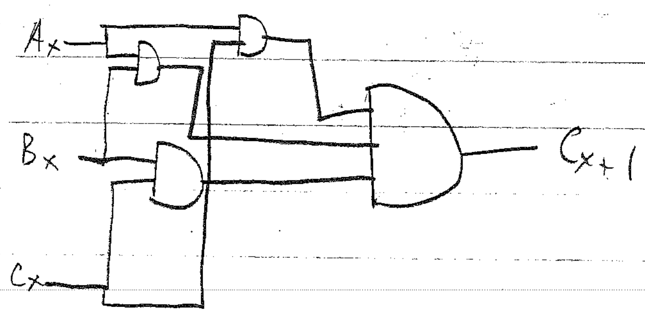
– confirmed

Part 4

It works! C_1 is the cin and C_4 is the cout — basically, if you have an extra base digit from your addition (eg. 1+01 has a cout from the ones digit (or a cin for the next digit)) you can pass it to the next circuit element.

You can connect multiple circuits in a row to add to higher bits by wiring the C_4 carry-out to the next circuit's C_1 carry-in.

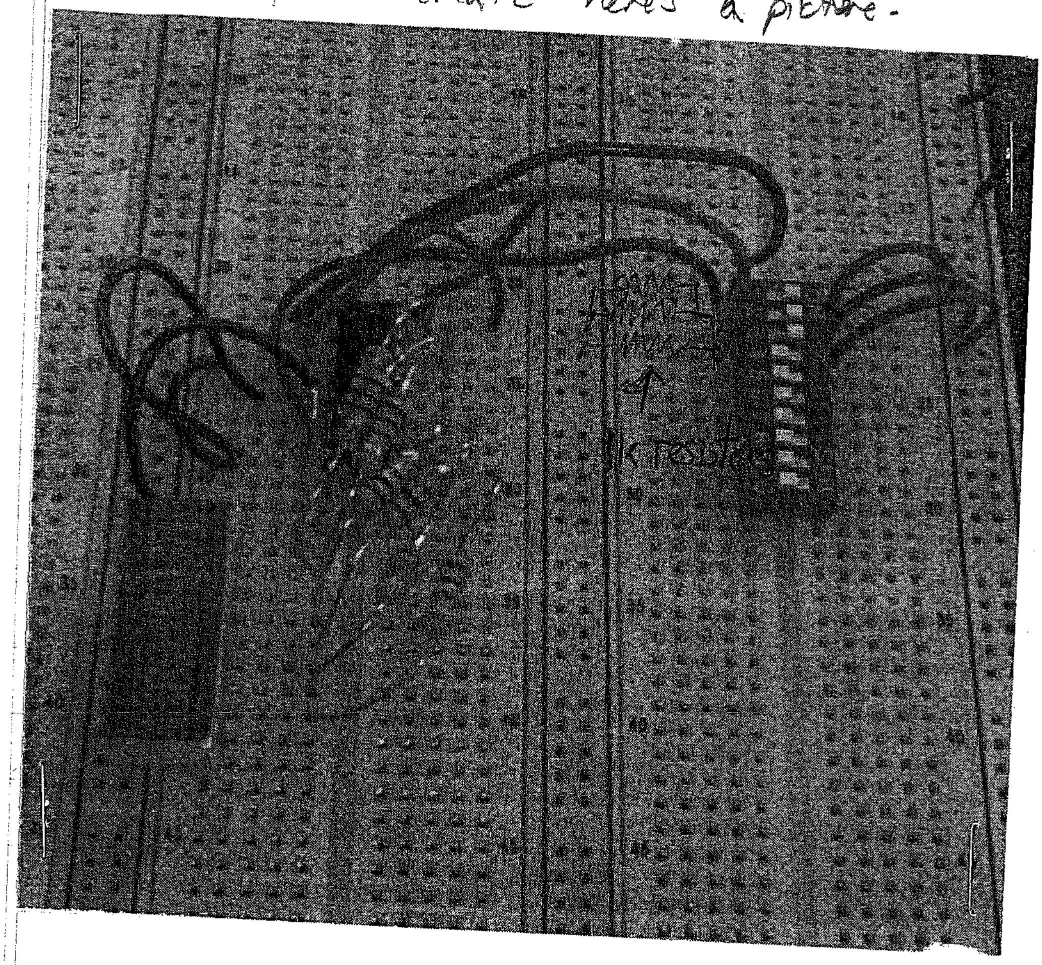




You can make an adder with these elements.

Part 5

I built the schematic - here's a picture:



At first, all of the LEDs were always on, until I realized that I needed to add parallel resistors to the DIP switch output to ground the output when the switch isn't on (these are the drawn-in resistors in the picture)

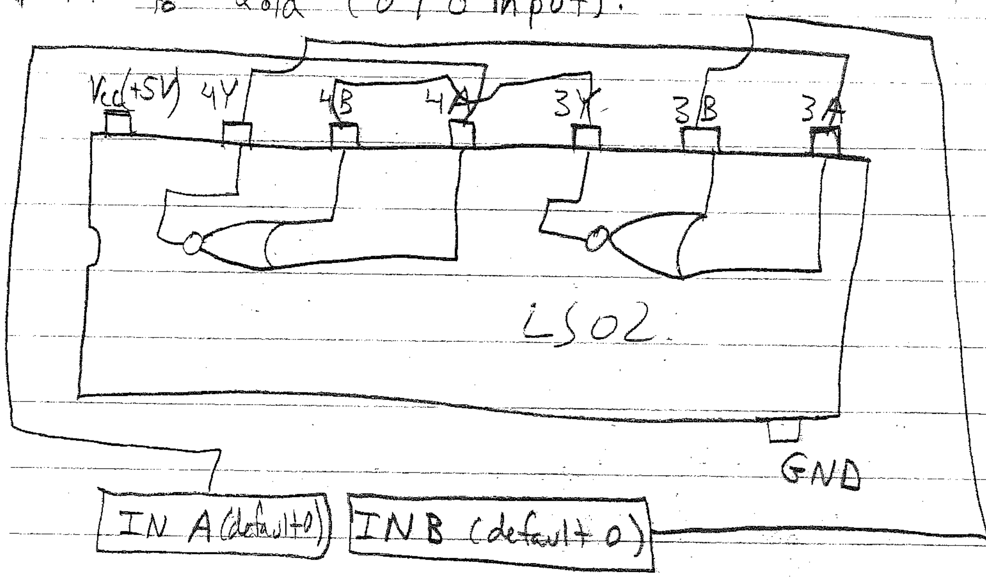
A_0	A_1	A_2	LED's
0	0	0	X O O O O O O O
0	0	1	O X O O O O O O
0	1	0	O O X O O O O O
0	1	1	O O O X O O O O
1	0	0	O O O O X O O O
1	0	1	O O O O O X O O
1	1	0	O O O O O O X O
1	1	1	O O O O O O O X

, where x = off and o = on (the inverse of what might be considered usual, since I didn't invert the output as specified)

Putting a 5Vpp square wave as the E_3 input, the corresponding output LED blinks at the input frequency.

Part 6

I built this circuit with two default-state-off DIP switches so that when neither was pressed the flip-flop would revert to Qold (0 / 0 input).



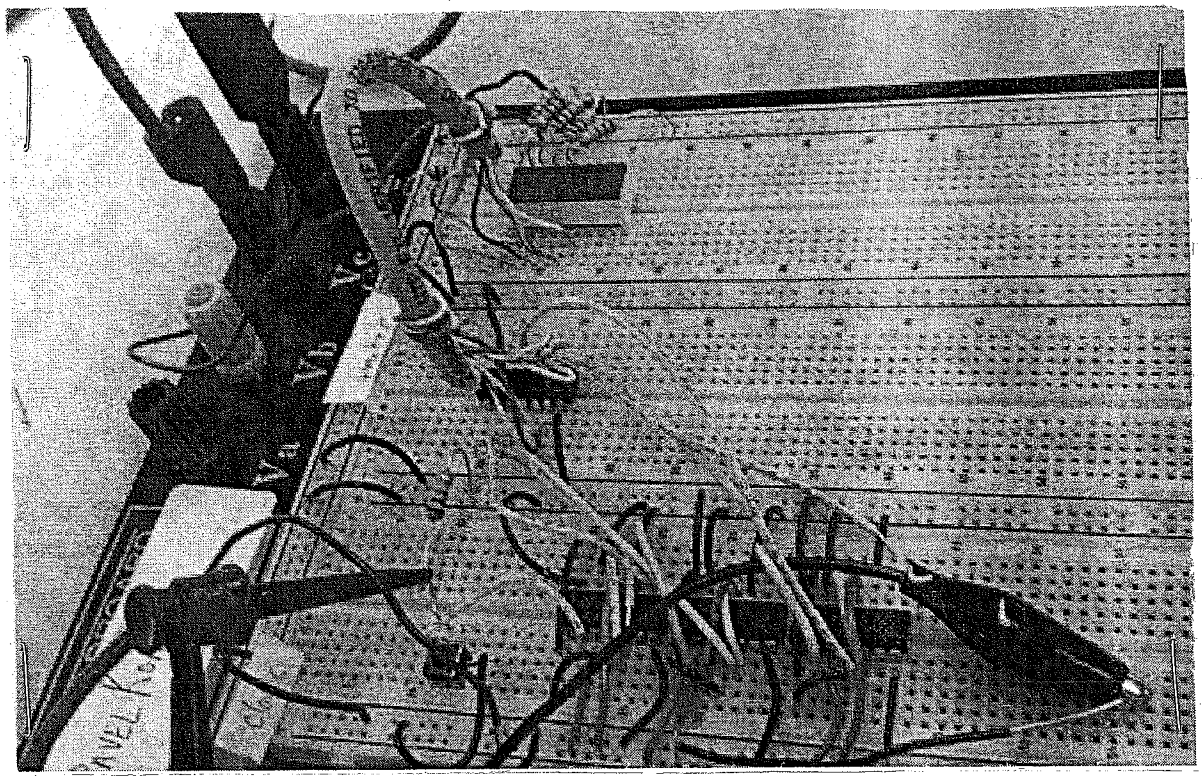
It was indeed the case that the default state remembered the last value.

what about the other cases

Draw circuit with the flip flops identified

Part 7

a) It works! Here's a picture: (note CAT5 connection cable)



b) also works!

Part 8

what was the shift register used?

a) The monolithic shift register is a single-chip version of the shift register I built in Part 7a. The LEDs dim sequentially.

b) The outputs count! To make a 8-bit counter, simply connect Ripple_carry_out to the clock in of the next 74LS164 chip, and then you'll have a 2x4bit = 8bit counter

Part 9

This does seem like a very useful discrete component for elongating a signal over time. I managed to keep an LED on for a period of time that was longer than instantaneous.