SVT-xxx
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Ghost-Track Removal Board

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I. Introduction

The original benchmark physics process for the SVT was $B \to \pi\pi$.[1] In this and other hadronic *B* decay channels, the level-1 trigger rates are enormous. That makes the SVT's background rejection and speed the primary considerations, with global track efficiency secondary. The 4-out-of-4 mode, in which a hit is required in each of four specified SVX layers, satisfies both of the primary requirements. However global track efficiency is hurt by the fourth power of the SVX single-hit efficiency.

When the Exotics and Top physics groups recognized the potential power of the SVT in furthering their physics goals, for example in studying Higgs associated production and $t\bar{t}$ production in the all-hadronic final states, they stressed the need for high track reconstruction efficiency for these rare processes. This prompted new SVT algorithms in which all five SVX layers are used, but only four hits are required for track reconstruction. The global track efficiency is indeed improved, but each track can produce a number of track candidates, either from different AM patterns or using different hits in the fit. The impact of the increased number of output SVT tracks on the level-2 decision time, and thus the maximum allowable level-1 trigger rate, can be large.

This proposal addresses the timing problem and provides additional benefits for the SVT system. Other solutions have been proposed, but we worry that they could reduce the flexibility of the SVT, flexibility that may well be needed once we have high luminosity running.

II. Board Functionality

The primary task of the ghost-track removal board is filtering out all but the one "best" SVT track corresponding to each XFT track. In a study of run I two-track-trigger data,[2] Tsuyoshi found that the expected mean number of roads in the most crowded phi sector is 5 for the 4-out-of-4 mode, but 30 for either of the two 4-out-of-5 algorithms being considered at that time. Implementing Tsuyoshi's suggestion that the 4-out-of-5 algorithm only be used for tracks above some $P_T^{\min}$ reduces the effect for most hadronic *B* decay triggers. However in events with high P_T jets such as the W/Z+H all-hadronic trigger, which has a 3 KHz level-1 rate, the effect of the 4-out-of-5 algorithm plus the combinatorics from multiple SVX hits in the road can make the number of track candidates very large. Transferring all of these across the level-2 Magic Bus and then sorting them out in the Alpha processor would be very time consuming. Even the dominant 40 KHz two-track hadronic *B* trigger could be helped by a ghost-track removal board, depending on how many of the 5 average roads pass the Track Fitter χ^2 cut.

We propose to build a board that would implement a simple but flexible algorithm for selecting the best track associated with each XFT track. The board would store a

maximum of one track for each of the 288 XFT linker chips, each of which covers a different ϕ region. As each track candidate enters the board from a Track Fitter, its "quality" would be found from a look-up table. The address would contain 9 bits: 5 bits of χ^2, the hit bits from layers 0 and 1, and the long cluster bits from layers 0 and 1. The look-up table output would be a number from 0 to 511, corresponding to the ranking of the track quality. If this were the first track candidate in that XFT ϕ region, it would be stored along with its quality ranking. If there already was another track candidate in that bin, then the new track would replace the previous one if its ranking were higher. Since the look-up table can be easily reloaded, the selection algorithm can be tuned as we get experience with run II data.

For diagnostic purposes, and as a fail-safe mode of operation, the board may be operated in pass-through mode, where all track candidates are passed to the level-2 processors.

We want to take advantage of this opportunity to add additional functionality that recent testing in B0 has shown to be useful. At present no SVT board implements the four level-2 buffers. Adding them to this board would allow readout into the event record of data currently accessible only through the spy buffer system, e.g. hit lists and road lists. Any SVT cable could be passed through the board to get its data into the data stream. This capability would also allow SVT tracks to be read out to validate the operation of the level-2 track interface board. It could also provide SVT readout if the level-2 decision crate were being used for other tests. Finally, this board would provide another path for the SVT to synchronize to the CDF clock for readout and receive L1A, L2B, and the bunch ID if the SVT were being exercised in its own partition. This would replace the functionality currently being provided by the unmaintainable hand modified Hit Finder board.

III. Board Architecture

In order to design the board quickly and have the greatest probability of success, we want to make maximum use of circuitry from existing Chicago CDF boards. Board construction will also be accelerated because many of the parts are already in our spares inventory. The VME interface, input logic (FIFOs, LVDS receivers), and output logic (LVDS drivers) will be copied from the Track Fitter board and the COT FADC board. The latter is a Chicago circuit currently being assembled that samples COT signals at 500 megasamples per second and feeds the results into the event data stream. The estimated cost of the VME interface is $50-100 per board.

We believe that processing can be handled entirely by a single Altera APEX 20K200-series chip. A fast version of this chip costing $325 is used on the COT FADC board. We could use a cheaper and slower version if it is readily available. The chip has 200K gates available for logic, four times a many as the Hit Finder clustering engine chip. This also adds to the flexibility in later changing the track selection algorithm. The chip also has over 100K bits of internal RAM, more than enough to hold one track for each of the 288 XFT ϕ regions plus the track quality look-up table. In fact simplistic bit counting indicates there might be room for an 11-bit look-up table, which could allow the hit bit and long-cluster bit from layer 4 to be added for example. We will gain experience with this chip starting in about a month when the FADC board testing begins.

The basic design consists of the VME interface, two connectors, some small parts, and one big chip. Since the SVT front panel has room for six connectors, it may make sense to triplicate the basic unit. This would reduce the latency of the filtering operation through parallel processing of different wedges and reduce the memory needed on each chip for track storage. It would also allow more pieces of the SVT internal data stream to be debugged when the board is used to insert SVT cable data into the event stream. And since we have twelve Track Fitters, and Mergers have four inputs and two outputs, one could elegantly capture the output of all twelve Track Fitters into three parallel inputs, just before the final Merger that feeds the level-2 track board.

IV. Schedule

The first task is to verify, using Quartus simulation, that the memory in a 20K200 chip can be arranged and used in the way we need for track storage and the look-up table. We also have to complete the parts list and quickly order any parts that do not overlap with other Chicago projects. The schematic will be assembled by starting with pieces of the Track Fitter and COT FADC boards. Layout, firmware design, and simulation will follow. The goal is a prototype delivered by April 1.

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[1] *SVT Technical Design Report*, cdf/doc/trigger/public/3108 (1994).
[2] *SVT with 5 SVX layers for the SVX-II*, T. Nakaya, cdf/run-II/trig/svt/stf/07 (1998).