Status of SVT Hit Finder Board and SVT Vertical Slice Test

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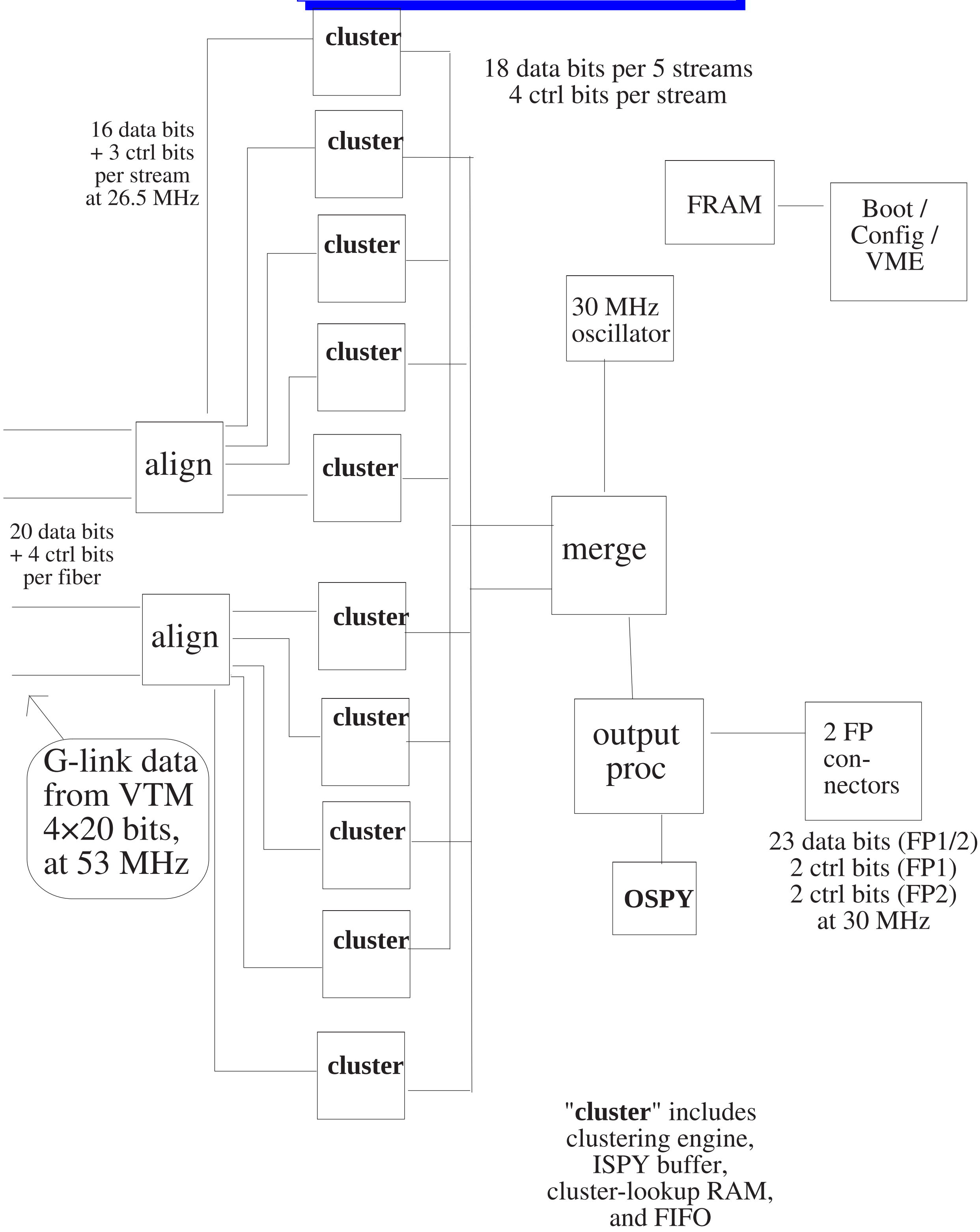


Prototype Experience

- Timeline
  - Jan 12: U of C internal design review
  - Feb 1: Sent Gerber files to Lugen
  - Feb 11: 4 PCBs back
  - Feb 17: 2 PCBs + parts to ADCO
  - Mar 25: 2 stuffed boards from ADCO
  - Apr 25: PCB review at FNAL (air flow issues; ID prom feature)
- Tested at U of C, FCC, B0 (details next page)
- Total of 3 assembly problems on 2 boards (ADCO): one at HCT buffer for internal VME data; two between P3 and alignment chip
- Use of board-level CAD simulation (QuickSim by Mentor Graphics) allowed us to fix many bugs well before prototyping stage and to understand behavior of large chips on real board
- Modularity and built-in diagnostics made check-out must faster
  - Spy memories as data source/sink
  - VME read/write access to FIFOs
  - Factorize testing of internal data processing; G-link input; output to downstream boards—stand-alone board test possible

Tests Completed

- VME I/O to all memories, FIFOs, registers
- Automatic load of firmware & memories from FRAM on power-up
- Current: when running, 5V $<$ 2A, 3.3V $<$ 5A
- Sent Ib beam data (few hundred wedge-events) from ispy to ospy; compared with calculation by C program to check internal logic
  - Ran on-board oscillator at 7.5, $\ldots$, 33.3 MHz (30 nominal)
- Sent same input from GSTM $\longrightarrow$ fiber $\longrightarrow$ VTM $\longrightarrow$ P3 $\longrightarrow$ HF, to check input stage of board
  - Ran GSTM at 50 MHz, 53 MHz, 55 MHz (53 is nominal)
  - Sent $\sim$ 4 GB through each of 4 fibers from GSTM to HF; checked HF output—no errors
- Sent same output to downstream SVT boards, to check board-to-board transmission
  - Checked "hold" (flow control) protocol with downstream board
- Incorporated into slice test at B0 with AMS, HB, etc.
- Checked backplane signals (SVT_INIT, SVT_FREEZE, CDF_ERROR, SVT_ERROR, SVT_LLOCK) with Spy Control board

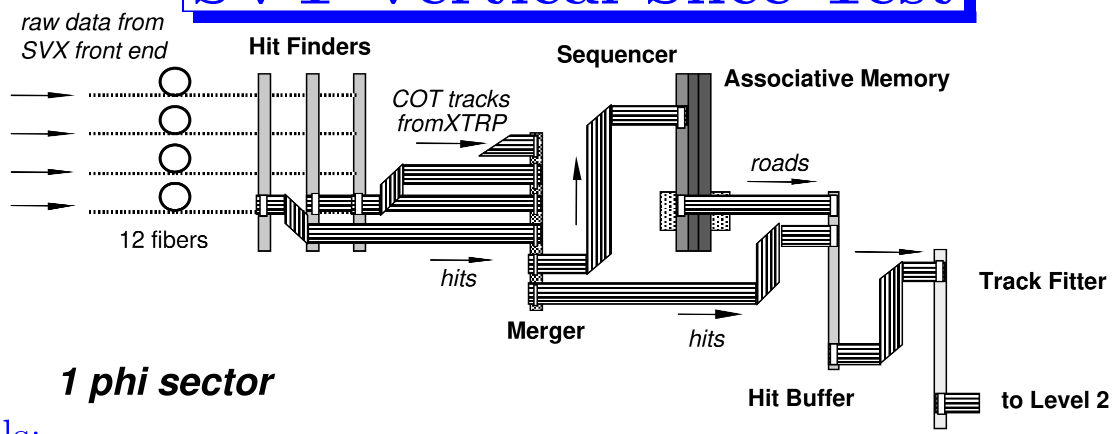
Status of Testing

- Board correctly receives, processes, and transmits data
- Comfortable with component choices. Have some speed margin and room for reconfiguration.
- Nearly all changes to date have been minor firmware mods. A few jumpers and pullups. Most embarrassing bug so far was reversing sense of several LEDs.
- Expect no changes to layout or routing of main components. Just gates, monostables, pullups. Altera pin assignments should be OK.
- Tests remaining are part of vertical slice test now underway (see later slides)
  - Long term tests overnight
  - Input from FIB (tried briefly in FCC with Petar)
  - In-situ monitoring & error handling
  - Full crate (e.g. many noisy VTMs)

Production Schedule

- Bid proces occurred in spring
- Selected SMT in Appleton, Wisconsin
  - UIUC had good experience with them
  - Same vendor will produce CrateSum, PreFred, TF
  - Harold visited a few weeks ago and likes their operation
- PO in the works. SMT should see $$ next week.
- Plan to give go-ahead next week to buy parts (same components as prototype)
- We continue VST, complete final design end of August
- **2–3 weeks** after we FTP Gerber files, we get 4 boards
- 2–3 weeks after we verify first 4 boards, remaining boards start to arrive (complete system needs 36 boards + spares)
- We are still ahead of any realistic schedule

SVT Vertical Slice Test



Goals:

- Test inter-board communication (e.g. loop at full speed, verify "hold" mechanism)
- Exercise system long term, high volume
- Emulate realistic conditions
  - Understand system initialization issues
  - Check output against simulation
  - Check timing against expectation
  - Develop monitoring/diagnostic software
- Check that we can detect & recover from errors
- Interface with SVX DAQ hardware, real fiber splitter rack, etc.

Existing VST Hardware

- One crate with PPC MVME

- (GSTM + fiber splitters as data source)

- Hit Finder† + VTM
- AM Sequencer†
- 2 AM boards† (with chips for 4K of 32K patterns)
- Hit Buffer†
- Spy Control (backplane signals, feedback to SRC)
- brief visit by Track Fitter†; will move in over next couple of weeks
  († = final prototype)

- very early Merger prototype
- real Merger later this summer
- XFT fanout in autumn

Tests in VST

- Inject various kinds of data:
  - Run Ib beam data
  - SVXII monte carlo
  - hits randomly drawn from a distribution
- Inject at various points:
  - Merger FIFO $\longrightarrow$ HB+AMS(+TF)
  - HF OSPY $\longrightarrow$ HB+AMS(+TF)
  - HF ISPY $\longrightarrow$ HF+HB+AMS(+TF)
  - GSTM FIFO $\longrightarrow$ VTM+HF+HB+AMS(+TF)
  - Soon also from FIB on first floor

  Most of these sources support both single burst and continuous loop
- Check output (in spy buffer) against simulation
- Expect to have realistic data (except XFT info) flowing all the way from FIB to TF by end of July
- Most tests so far send $\sim$ 1 msec of data then check result. Work in progress on system to sample pipeline in real time & compare with simulation—needed for real running!

VST Summary

- A good fraction of a slice of SVT is already present
- Number of board types participating in test still growing
- Tests are becoming more realistic
- Good opportunity to understand SVT software requirements
- Slice test is a great opportunity to understand system-level issues. Seems prudent to learn as much as we can before starting board production.