Level 2 Magical Mystery Board
Preliminary specification
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The L2MMB will be a CDF-style 9U VME transition module designed to emulate the Magic Bus I/O of a Level 2 Alpha processor, in order to act as a diagnostic data sink for Level 2 interface cards. Data collected from the Magic Bus will be transmitted to an SVT cable. SVT cable data can be monitored using the spy buffers of an SVT Merger board, read into the event using a L2/Track board, or transmitted to a separate Level 2 decision crate for testing or prototyping. Analysis of Magic Bus data with a logic analyzer will also be straightforward. It is, of course, possible to put the SVT-format data back onto a Magic Bus, using the MB side of a L2/Track board; the L2MMB is essentially the inverse of a L2/Track board.

The L2MMB will provide a simple, inexpensive Magic Bus data sink, with several applications.

Test Stands: It is not currently feasible to provide a Level 2 Alpha processor to each of several (FNAL ×2, ANL, Michigan, UCLA) test stand sites. As a result, many tests that could be performed in test stands must instead be done in situ.

Parasitic Readout: It may be convenient, especially during commissioning, to allow the output of one or more not-fully-tested interface boards to be read into the CDF event without jeopardizing the smooth operation of the trusted subset of Level 2.

Partial Factorization: On a shared bus, a given board may receive, process, and transmit data correctly, but somehow disrupt the correct operation of other boards on the bus. The L2MMB will enable data collection from several sources to proceed on separate Magic Buses, if necessary.

Complete Factorization: A more extreme form of factorization would place every interface board's data on its own private Magic Bus, thereby eliminating all bus arbitration issues. This could be done with a TDC backplane, in which each slot is essentially a straight-through Magic Bus, and one L2MMB per interface board. (The four RECES boards would be read on a Magic Bus, using slow single-word transfers, and the L1 bits would be handled as a special case.) The data from an arbitrary number of L2MMBs can be fanned into a single SVT cable with one or more SVT Merger boards (four inputs, two identical outputs).

Data Reduction: Using a versatile FPGA, simple firmware algorithms could be applied to Level 2 data, e.g. to reduce the volume of data transmitted to processors or to detect in hardware various error conditions. (Some interesting data reduction may be possible if e.g. the L1 bits or XTRP track list is available on a spare SVT input connector. This idea should be saved for a rainy day.)

Test Stand Relevance: It has been argued that a complete Level 2 test stand may never be realized, as it is difficult to reproduce exactly the effect of every board on every other board in the Level 2 decision crate. In the event that one or more boards work properly in a test stand but not on a fully loaded bus, those boards' readout can be factorized (as described above), making in-situ operation identical to test stand operation. It follows that an arbitrary set of interface cards can be made to work together if (a) each card works separately with the L2MMB and (b) a single L2/Track board works with the Alpha.

Parasitic Upgrade: Changes in the computing industry since Run 1 make it likely that CDF will need to commission the next generation of Level 2 processor some time before the start of Run 2b. The L2MMB will allow a separate processor to spy on the full Level 2 data stream non-invasively, for validation against the Alpha's decisions. The same argument could apply to a spare or newly repaired Alpha board.

While the SVT cable (23-bit-wide LVDS data at 30 MHz, plus data strobe and flow control) may not be the first choice for a newly designed protocol (e.g. one may prefer 32 data bits), it brings for free SVT's extensive diagnostic, readout, and data source/sink hardware and software. It also offers bandwidth (86 Mbytes/sec) comparable to the full Magic Bus bandwidth (80-160 Mbytes/sec). Finally, LVDS components are inexpensive, easy to use, and likely to remain available for some time.

Details: The L2MMB will consist of a bi-directional Magic Bus interface, a large Altera chip (probably APEX 20K200 in a 356-pin BGA package), a 60 MHz oscillator, and the LVDS circuitry (six quad driver chips, one receiver chip) needed for an SVT output cable. CDF-specific J2 backplane signals will also be connected, including at least CDFCLK, B0, L1A, L2B0, L2B1, HALT, RECOVER. One HP logic analyzer header (16 bits plus clock) will provide debug data. The board will be programmable via JTAG.

The L2MMB will function in three modes: target, master, and spy. In target mode, it will appear as a Level 2 Alpha now appears to a L2/Track, Cluster List, IsoList, or L1/L2 board. Once the L2MMB asserts STLOAD in response to L1A from the TRACER, the interface board will acquire the single-slot "bus" and send its data to the L2MMB. The L2MMB will buffer the data in a FIFO (within the Altera chip's internal SRAM), then forward them to the SVT output cable, respecting the flow-control signal of the receiving SVT board. Each event's data will be tagged with a programmable header identifying the L2MMB instance and a trailer indicating the bunch counter number and L2 buffer number of the event. In master mode, a state machine within the L2MMB will acquire control of the Magic Bus, then issue a sequence of programmed I/O transfers, e.g. from a RECES or L2/Muon board, then send the data to the output cable. In spy mode, the L2MMB will passively observe transfers initiated by other Magic Bus masters, recording address and data values into its FIFO on each data strobe. Note that the SRAM (FIFO) capacity of an APEX 20K200 is 13 Kbytes, while the data sent to the Alpha per event are typically a few hundred bytes.

TBD: We need to check that using TDC backplane as single-slot Magic Bus will really work. We need to understand best choice of transceiver chips (e.g. ABTE vs FCT). We need to study the Alpha's Magic Bus interface. We need to understand how best to handle arbitration lines, e.g. for single-slot operation. We should probably provide a simple (but slow) interface to a PC's parallel port, for control and debug functions. Is there any motivation to provide an SVT input connector (e.g. for control data, for daisy chaining, or for data whose presence would allow easy sparsification of interface board data)?

Counting Pins: The preferred Altera chip has 277 I/O pins available.

MBDATA(128), MBADDR(32), RD/WR*, DSTROBE*, DDONE*, DONE_OUT
MBRESET*, START_LOAD*, BUFFER(2)

EV_LOADED(4), AP_FIFO_EMPTY(1) are O/C output

BOSS, BOSSREQ, BOSSGRIN, BOSSGROUT are PECL (Need both receive and drive? Use jumpers or test points for easy access! Do we have any need for normal arbitration circuit?)

Probably don't need MOD_DONE(19)?

On-board 60 MHz clock

Debug(16), DebugClk

CDFCLK, B0, L1A, L2B0, L2B1, HALT, RECOVER

Are BC, L1R, L2A or others needed?

SVT DOUT(23), DSOUT, HOLD_IN

Spare I/O pins and buffer chips to connect to a PC parallel port?

Option for SVT input connector as well as output? (Would be 25-30 pins.)

Total: min is 227, max is close to the limit of 277