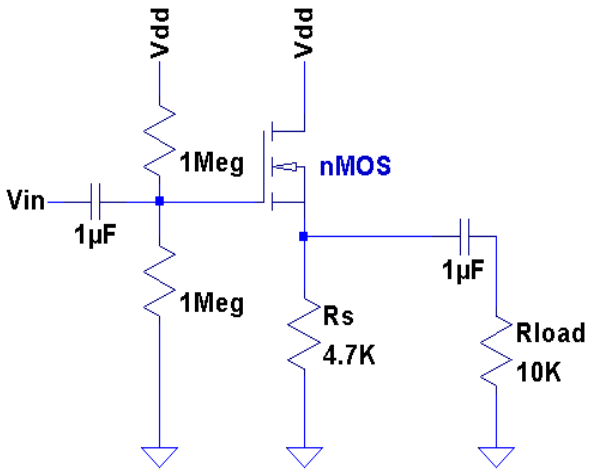
**Physics 364 – fall 2010 – Lab #7 – due by lecture, Monday 2010-11-01**

Lab #7 is the last of three transistor labs. This week, we look at Field Effect Transistors. After seeing that FETs can be used in many of the same circuits we are used to building with BJTs, you will move on to building two simple logic gates as a transition into the digital part of the course that starts next week. In Thursday's culmination of Lab #7 (some of which may be handed out on Thursday), you will build a simple FET-based amplitude modulator, allowing you to transmit a signal to a nearby AM radio.

## Part 1: nMOS source follower

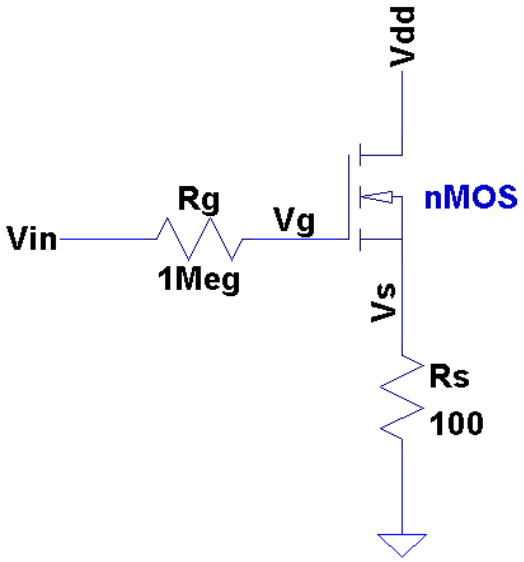
Build the nMOS source follower shown to the right, using , and Vdd=+15V. A source follower is the FET equivalent of an emitter follower. (Remember that emitter, base, and collector are analogous to source, gate, and drain.) Convince yourself that the FET's input resistance is very large. The load resistor is present merely to demonstrate that the follower's output impedance is much smaller than its input impedance – since it wouldn't be much use as a follower otherwise. Try removing it or varying it to see whether its presence affects the output amplitude.




A few points for your information (i.e. not part of the lab): If we had built this follower with a depletion-mode FET, e.g. a JFET, then $I_{DS}$ would be appreciable when $V_{GS}$=0, making the biasing network unnecessary. (A very large resistor to ground would suffice.) So in fact many opamps and instruments use JFET inputs. A JFET is also far less susceptible to damage from static electricity than a MOSFET, because its gate is a reverse-biased semiconductor layer, while the very thin gate of a MOSFET is electrically insulated from the substrate. But MOSFETs are the building blocks of CMOS digital logic, as well as many analog switches, and there are only so many topics we can cover in one semester! An n-channel enhancement-mode MOSFET is the nearest FET cousin to the NPN BJT, so is a good starting point for learning about FETs.

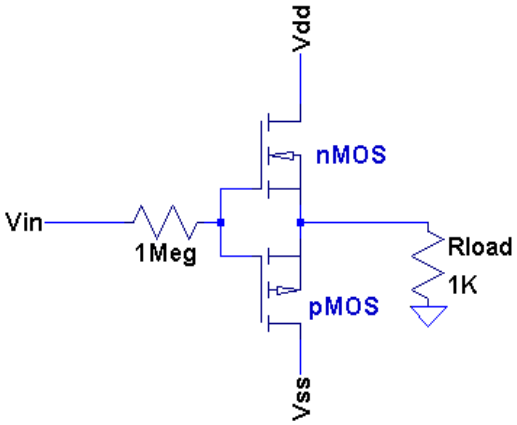
## Part 2: MOSFET characteristics

Build the circuit shown at right, which will allow you to measure the turn-on curve of $I_{DS}$ vs. $V_{GS}$, by analogy with the BJT measurements you made in Lab 5. Use Vdd=+15V (though you can try other values to vary $V_{DS}$), and drive Vin from your +6V DC supply. Measure Vg and Vs vs. Vin and estimate Ids vs. Vgs. Also, see whether you can see any evidence of gate current. What is $V_T$, the threshold Vgs at which Ids starts to rise? Graph Ids vs. (Vgs-Vt). The curve should be quadratic, in sharp contrast to the exponential rise of a BJT's collector current with Vbe. The data sheet lists a wide range of $V_T$, from 0.8—2.4V. This large part-by-part variation is typical of FETs.



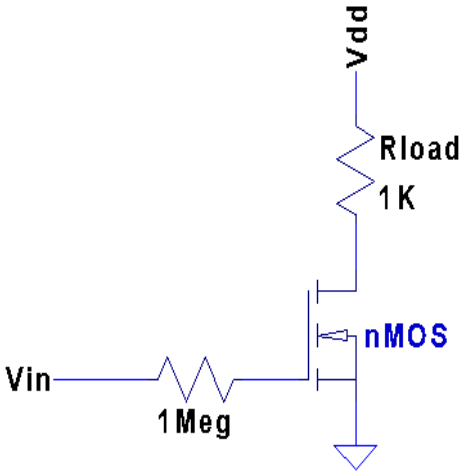
**Part 3: CMOS push-pull follower**

Build the CMOS push-pull follower shown at right, using one nMOS and one pMOS FET. Use Vdd=+15V, Vss=-15V. Drive Vin with a sine wave several volts in amplitude. Because of the large $V_T$, the crossover distortion will be quite noticeable. Looking for a voltage drop across the 1M resistor, do you see any sign of nonzero gate current?



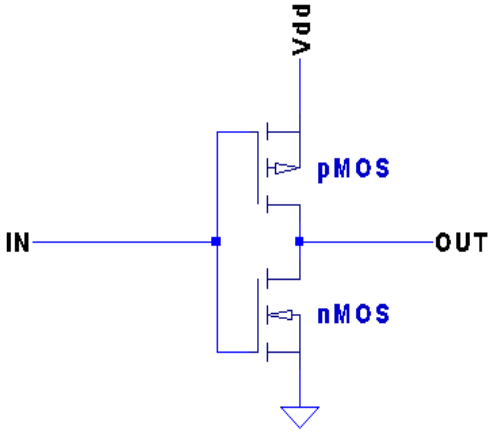

**Part 4: NMOS switch**

Build the NMOS switch drawn to the right. Use Vdd=+15V. Try connecting Vin alternately to ground and to Vdd, to turn the switch off, then on. With the switch on and off, measure the voltage at the drain to estimate the current through the load resistor. You might also measure the voltage at the gate to see whether there is any gate current. (Don't be fooled by the 10M input resistance of your DVM when looking for a voltage drop across the 1M resistor.) Try to estimate the "on" resistance of the FET, i.e. the resistance from drain to source when Vgs >> Vt, by measuring Vd.




**Part 5: CMOS inverter**

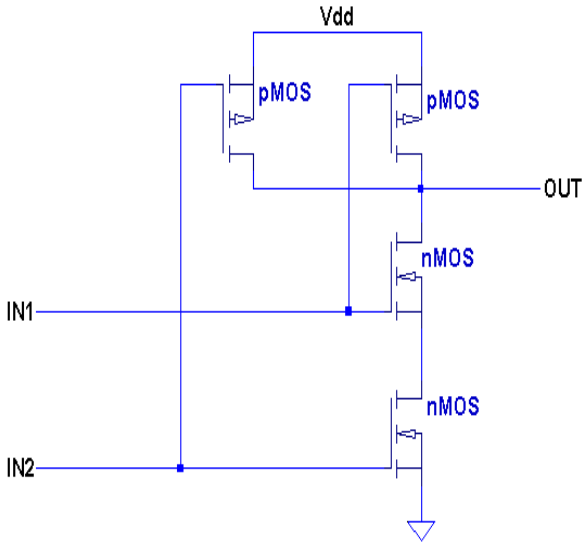
Build the CMOS inverter shown at right, using Vdd=+5V. It is basically an upside-down version of the CMOS push-pull. (Note that the pMOS transistor is on top here, and on the bottom in the push-pull.) Connect Vin alternately to Vdd and to ground, and look at Vout. What is the resistance from Vdd to Vout in the ON state? What is the resistance from ground to Vout in the OFF state? Find a way to measure the current drawn from Vdd (i.e. to infer the power consumption) when this gate is held in the ON state, when it is held in the OFF state, and when it is switching states. (For example, you can drive Vin with a square wave between 0V and +5V, and put a resistor between the inverter and Vdd to look for current flow.) CMOS logic gates are known for using negligible power except when switching states.




The idea of logic gates, which we will discuss in much more detail next week, is that (for instance) +5V represents TRUE or 1, while 0V represents FALSE or 0, and gates perform logical operations.

**Part 6: CMOS NAND gate**

Build the CMOS NAND gate shown to the right, and show that it performs the NAND operation, where +5V (=Vdd) represents TRUE, and 0V represents FALSE. Sketch the ON/OFF states of the four FET switches, note Vout, and note the voltage at each drain, source, or gate (of the FET) for each of the four possible input states.




A NAND gate takes two logical (i.e. TRUE/FALSE) inputs, A and B, and outputs NOT (A AND B). In C, this is !(A&&B), and in formal logic, this is ¬(A^B). You might think (as I once did) that it is stupid to make NAND gates when you could make more intuitive AND gates instead. The ingenious thing about a NAND gate is that it can be wired up to make an inverter. So NOT (A NAND B) gives you (A AND B). And ((NOT A) NAND (NOT B)) gives you A NOR B. And NOT (A NOR B) then gives you (A OR B). So with a NAND gate, you can do it all.

**Part 7: sample & hold using CMOS analog switch**

This exercise will use a CMOS analog switch to form a "sample and hold" circuit, which permits you to hang on to the instantaneous state of an input signal while you record it (usually with an analog-to-digital converter). The details of this part of the lab will be filled in by Thursday, once I find out whether we will use the DG403 (preferred, but not in stock yet) or the CD4066BC (in hand now). The preferred part has a lower ON resistance and is a "single pole, double throw" switch, meaning that it can easily multiplex one output between two inputs – which is often a handy feature to have.

**Part 8: variable resistor / modulator**

This exercise will explore the "linear" region of a MOS FET, i.e. small $V_{DS}$, in which $I_D$ varies approximately linearly with $V_{DS}$. (In the FET's "saturated" region, which confusingly corresponds to the BJT's "active" region, $I_D$ is nearly independent of $V_{DS}$.) The linear region can be used to create a voltage-controlled resistance. This can be used, for instance, to change the gain of an amplifier under the control of a computer. One fun application of a voltage-controlled resistance is to make one signal modulate another one. Your function generator knows how to do this by itself, but here the modulation will be under the control of your own circuit. Using amplitude modulation, you should be able to transmit a signal to a nearby AM radio. The details of this part will also be worked out before Thursday.