Physics 364, Fall 2014, Lab #14 **Name:** ____________________

(transistors III: differential amplifier; push-pull buffer; and switch)

Monday, October 20 (section 401); Tuesday, October 21 (section 402)

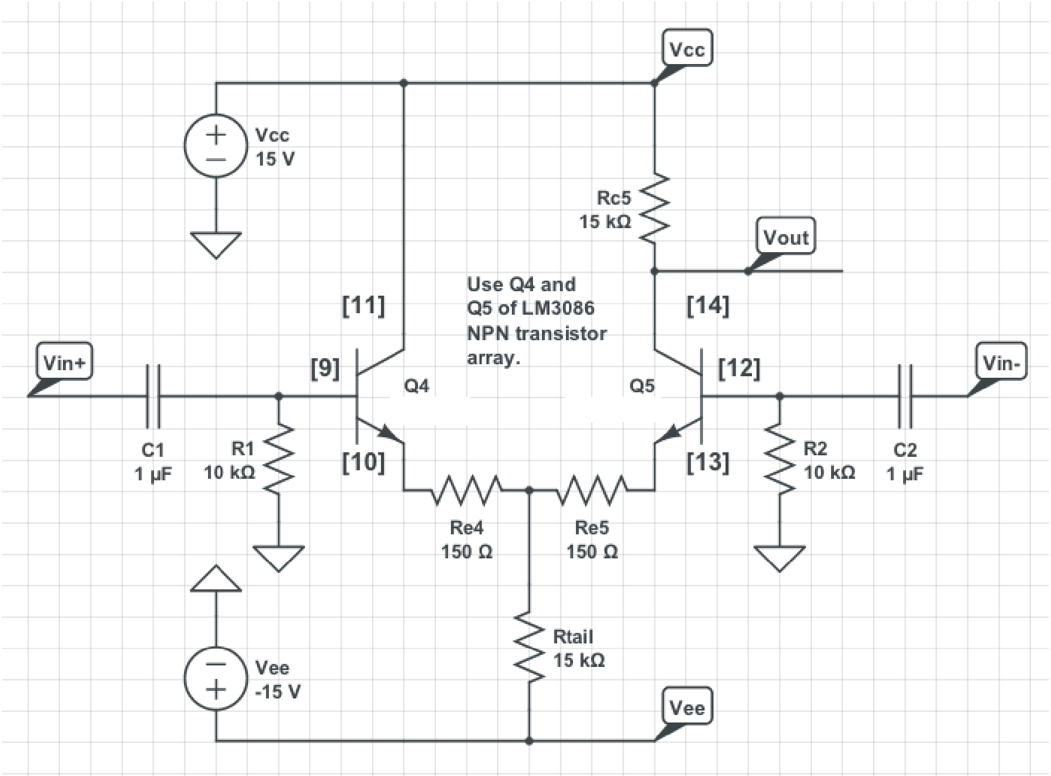
Course materials and schedule are at `positron.hep.upenn.edu/p364`

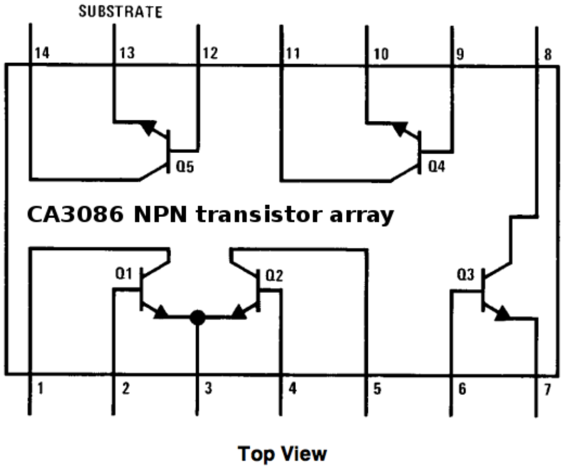
Today's is the third of four labs covering Bipolar Junction Transistors. Today, we will study the *differential amplifier* and the *push-pull buffer*. In the next lab, these two circuits will form the input and output stages, respectively, of our home-made opamp. Finally (if you have time left at the end, and if you didn't already do it last week), we'll use a transistor as a simple on/off *switch,* which is a non-linear application of the transistor's useful property of permitting a very small current to control the flow of a much larger current.

Part 1 **Start Time:** ________________

differential amplifier (time estimate: 90 minutes)

Use transistors Q_4 and Q_5 from a CA3086 NPN transistor array to to build the differential amplifier shown below. Numbers in square brackets indicate pin numbers on the 3086 array. The pin assignments for the 3086 array are shown in the chip diagram below. (All of the transistors are NPN, but Q_4 and Q_5 are drawn upside-down in the chip diagram.) Remember that pin numbers go counterclockwise, starting from the lower left. The reason we are using this transistor array is that the transistors are well matched to one another by the manufacturer; also, having the two transistors on the same piece of silcon keeps them at the same temperature, so that they behave symmetrically.





We've AC-coupled the inputs of this amplifier mainly to reduce the odds of cooking the transistors. In practice, one big advantage of this differential-amplifier circuit is that it is easy to use with DC-coupled inputs. (It doesn't require the annoying biasing network found on the common-emitter amplifier.) So one sometimes sees this circuit used, with one input grounded, to amplify a single DC-coupled signal.

1.1 First calculate the expected common-mode gain of this amplifier. (I worked out a similar circuit in the notes.) How would you go about measuring the common-mode gain? Give it a try, by sending the same 1 $\mathrm{V_{pp}}$ sine wave into each of the two inputs, and then looking at the output. Does your measurement agree with your calculation? (In this case, you might find it convenient to use the "AC coupling" feature of the oscilloscope to look at V_{out}, in order to subtract the large DC offset.)

(Blank page, in case you need space to think.)

1.2 Next calculate the expected differential gain of this amplifier. The easiest way to send a differential signal into the amplifier is to send a signal into only one of the two inputs, leaving the other input grounded. (Ideally, to measure only the differential gain, we would send equal and opposite signals into the two inputs. But the differential gain is so much larger than the common-mode gain that the easier technique will work for us.) Does the differential gain agree reasonably well with your calculation? You'll probably need to make the input voltage quite small for this measurement.

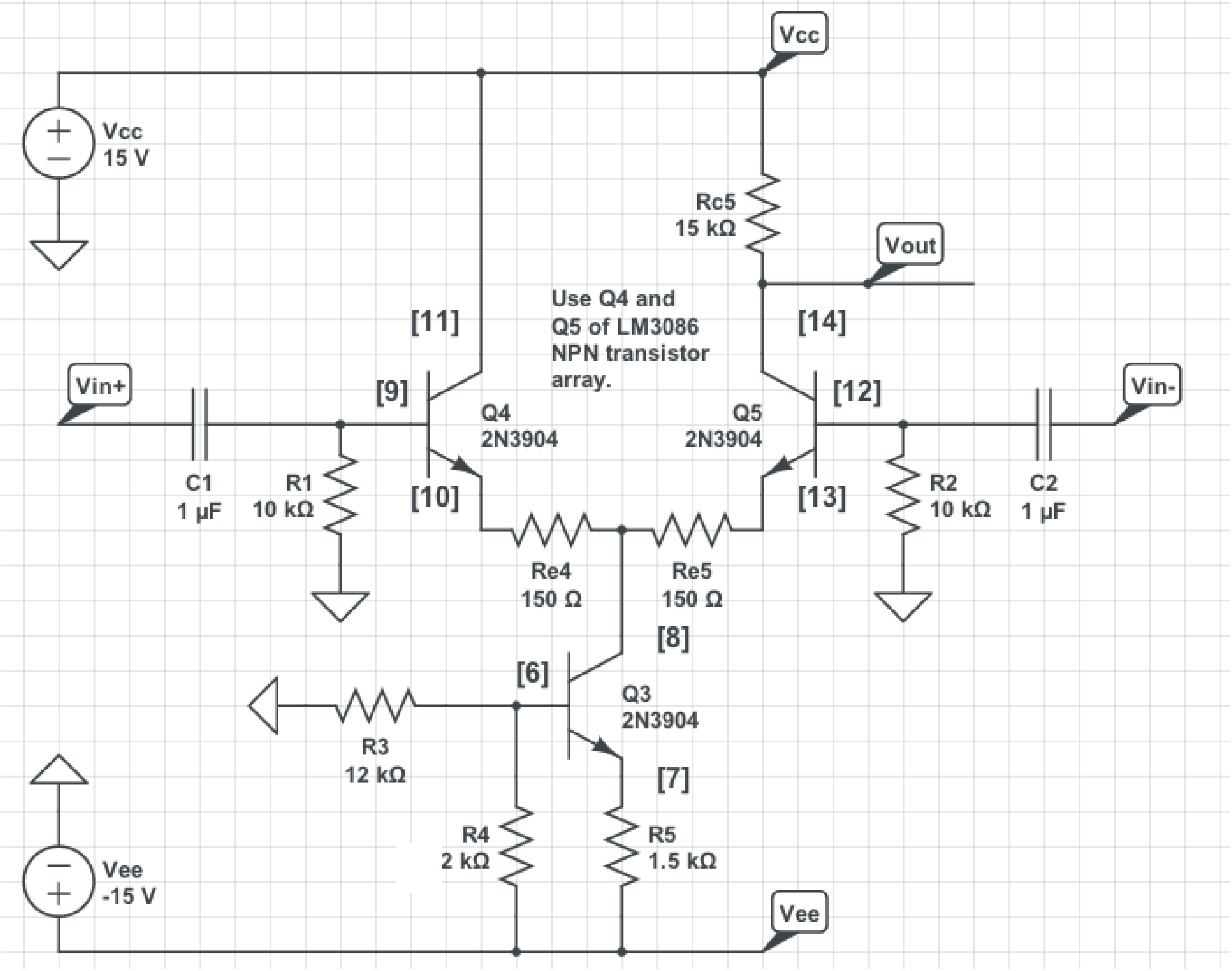
(Blank page, in case you need space to think.)

1.3 Now use Q_3 of the transistor array (pins 6 (base), 7 (emitter), and 8 (collector)) to replace R_{tail} with a simple transistor current source, as shown in the figure below. This current source is of the same basic design you studied in Lab 13. Make the argument that it should function as a 1 mA current source.

An ideal current source would have an output resistance $R_{\text{out}} = \infty$, which would reduce the common-mode gain to zero. In reality, this current source made with this model of transistor will have $R_{\text{out}} \sim 3\ \text{M}\Omega$, according to my CircuitLab simulation

`https://www.circuitlab.com/circuit/3m3emx/lab14-part1_3-current-source/`

which will make the common-mode gain very small but still nonzero. Estimate roughly how small you now expect the common-mode gain to be, and then confirm that it is indeed very small by driving both amplifier inputs simultaneously with a 2 V_{pp} sine wave, and checking that the effect of this sine wave on V_{out} is barely detectable (or perhaps undetectable). Finally, unplug the sine wave from one of the two inputs just to confirm that the differential gain is still quite large and that the amplifier is still alive.



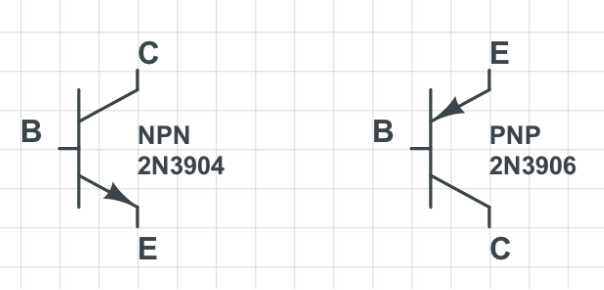
(Blank page, in case you need space to think.)

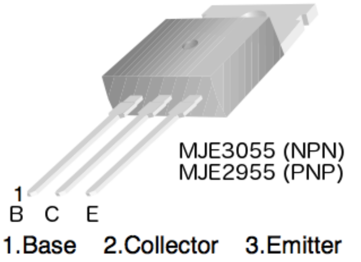
(Blank page, in case you need space to think.)

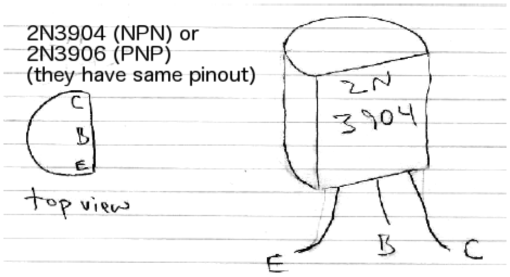
Part 2 **Start Time:** ______________

push-pull buffer (time estimate: 60 minutes)

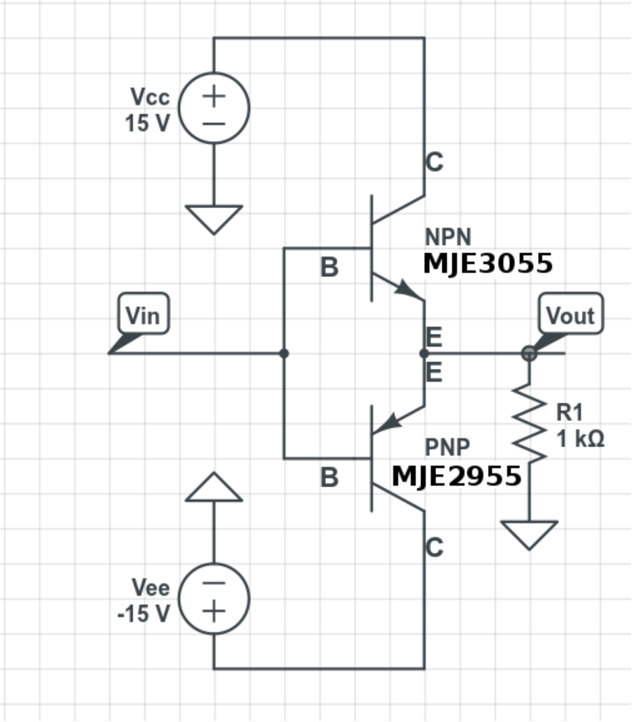
This is the first time you will use a PNP transistor in this course, so we'll show you below what one looks like. For a PNP transistor, the arrow on the emitter points toward the base, vs. away for an NPN transistor, and usually the emitter is drawn above the collector (to represent higher potential) for the PNP case. The 2N3904 (NPN) and 2N3906 (PNP) are comparable NPN and PNP transistors that have the same appearance and pinout. We also have the MJE3055 (NPN) and MJE2955 (PNP), which are designed for higher power. Note that the MJE3055/2955 pinout differs from the 2N3904/3906 pinout. We will use the higher-power transistors for the push-pull buffer because they will allow us to send a larger (louder) signal into your speakers, which will be more fun!





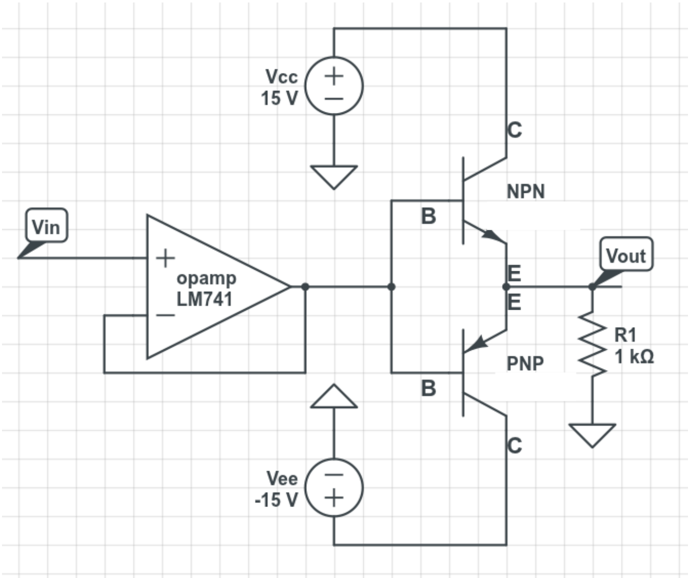


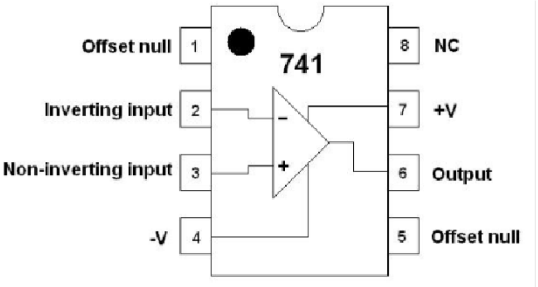
2.1 Build the push-pull buffer shown in the figure below, using one MJE3055 (NPN) transistor and one MJE2955 (PNP) transistor.



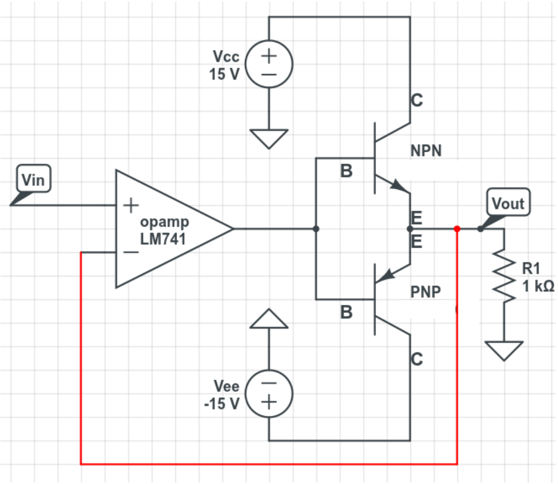
Drive your push-pull with a 5 V_{pp} sine wave, and look at V_{out}. Use a 440 Hz sine wave (corresponding to the *A* note above middle *C*) so that you don't annoy your neighbors too much with the irritating sound of the usual 1 kHz sine wave. Do you see the crossover distortion on the scope, when the output crosses zero? Why does this happen? Also explain why the high and low points of V_{out} are about a diode drop closer to 0 V than the high and low points of V_{in}. Now try driving a speaker with V_{out} so that you can hear the distortion with your own ears. (Connect the two terminals of the speaker between V_{out} and ground, i.e. in parallel with the 1 kΩ resistor.)

2.2 Now put an op-amp follower between the signal source and the push-pull, as shown in the figure below. This should do exactly the same thing as the circuit in part 2.1, but testing it this way gives you a chance to check that you wired it up correctly.





2.3 Now move the feedback to the output of the push-pull, as shown in the figure below. You should see the crossover distortion magically disappear! Why does this happen? Try both to see the distortion disappear (with the scope) and to hear it (with the speaker). You can make it come and go by moving the feedback point back and forth. Another thing that the opamp feedback corrects is the reduced amplitude of V_{out}. How does the opamp accompish this amazing feat? To get some idea of what the opamp is doing, use one scope probe to observe the point between the opamp and the push-pull (i.e. where the opamp's output meets the two transistors' bases), and see what the opamp is doing to "undistort" the waveform! The opamp output pin's "undoing" of the push-pull's distortion is somewhat amazing to watch.



(blank page — in case you need space)

Part 3 **Start Time:** ________________

on/off switch (optional – if time) (time estimate: 30 minutes)

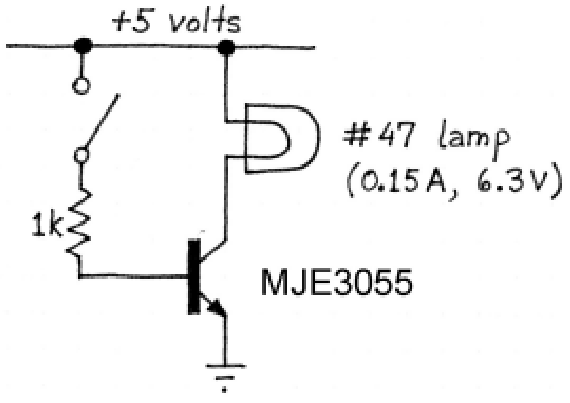
The key feature of a transistor is that it allows a small current (I_B) to control the flow of a much larger current (I_C). So far we have used this feature to make amplifiers whose output is proportional to the input, but larger — larger current in the case of the emitter follower, and larger voltage in the case of the common-emitter amplifier.

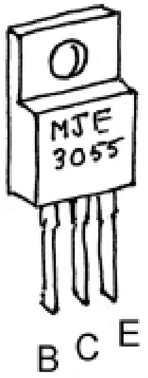
A transistor can also be used as an electrically controlled on/off switch, in which the presence of absence of a relatively small current (I_B) switches on or off the flow of a much larger current (I_C). When the switch is *off,* the transistor is in *cutoff* mode, where $I_C = 0$. When the switch is *on,* the transistor is in *saturation* mode, where V_{CE} is small (typically a few tenths of a volt above zero), $V_{BE} > 0$, and I_C is large. In this mode, $I_C \neq \beta I_B$. The motivation for using saturation mode is that the power $I_C V_{CE}$ dissipated in the transistor is small, even though a large current I_C flows through the load that the transistor is turning on/off (and hence through the collector).

Try buildling the transistor switch shown below. Use a high-power MJE3055 transistor from the back room: it can tolerate larger currents and can transfer heat to the surrounding air more effectively than the smaller 2N3904. **Notice the different pinout!** Use a pushbutton DPDT switch from the back room to switch the small current I_B on/off. (Or just use a wire if you're feeling lazy.)

Measure (or infer) I_B. Measure I_C and V_{CE}. Convince yourself that I_B, while significant, is still quite a bit smaller than I_C in saturation mode.

To convince yourself that I_C is no longer proportional to I_B in the saturated regime, try replacing the 1 kΩ resistor with 10 kΩ. The ≈ ×10 reduction in I_B should make only a very small difference in I_C. So "saturated" means that the transistor is as "on" as it can be: that further increases in I_B (the control knob) will not appreciably increase I_C (the flow that is being controlled). Saturation mode is like the fully-open state of a valve.





(Blank page.)

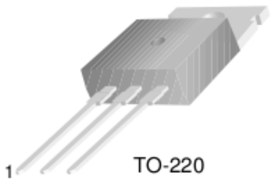
FAIRCHILD
SEMICONDUCTOR™

MJE3055T

MJE3055T

General Purpose and Switching Applications

- DC Current Gain Specified to I_C =10A
- High Current Gain-Bandwidth Product : f_T = 2MHz (Min.)



1.Base 2.Collector 3.Emitter

NPN Silicon Transistor

Absolute Maximum Ratings T_C=25°C unless otherwise noted

Symbol	Parameter	Value	Units
V_{CBO}	Collector -Base Voltage	70	V
V_{CEO}	Collector-Emitter Voltage	60	V
V_{EBO}	Emitter-Base Voltage	5	V
I_C	Collector Current	10	A
I_B	Base Current	6	A
P_C	Collector Dissipation (T_C=25°C)	75	W
P_C	Collector Dissipation (T_a=25°C)	0.6	W
T_J	Junction Temperature	150	°C
T_{STG}	Storage Temperature	- 55 ~ 150	°C

Electrical Characteristics T_C=25°C unless otherwise noted

Symbol	Parameter	Test Condition	Min.	Max.	Units
BV_{CEO}	Collector-Emitter Breakdown Voltage	I_C = 200mA, I_B = 0	60		V
I_{CEO}	Collector Cut-off Current	V_{CE} = 30V, I_B = 0		700	μA
I_{CEX1} I_{CEX2}	Collector Cut-off Current	V_{CE} = 70V, V_{BE}(off) = -1.5V V_{CE} = 70V, V_{BE}(off) = -1.5V @ T_C = 150°C		1 5	mA mA
I_{EBO}	Emitter Cut-off Current	V_{EB} = 5V, I_C = 0		5	mA
h_{FE}	*DC Current Gain	V_{CE} = 4V, I_C = 4A V_{CE} = 4V, I_C = 10A	20 5	100	
V_{CE}(sat)	*Collector-Emitter Saturation Voltage	I_C = 4A, I_B = 0.4A I_C = 10A, I_B = 3.3A		1.1 8	V V
V_{BE} (on)	*Base-Emitter On Voltage	V_{CE} = 4V, I_C = 4A		1.8	V
f_T	Current Gain Bandwidth Product	V_{CE} = 10V, I_C = 500mA	2		MHz

* Pulse test: PW≤300μs, duty cycle≤2% Pulse

Typical Characteristics

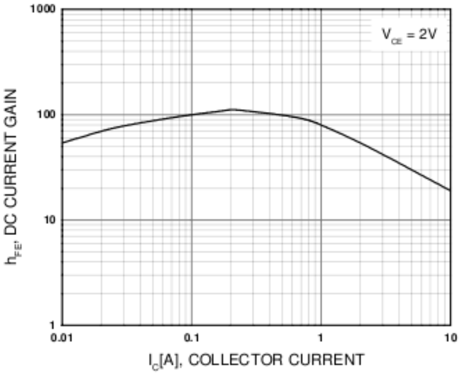


Figure 1. DC current Gain

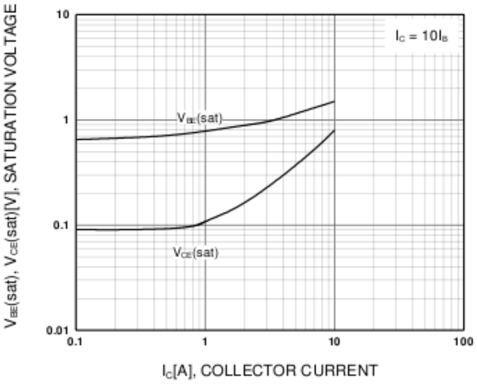


Figure 2. Base-Emitter Saturation Voltage Collector-Emitter Saturation Voltage

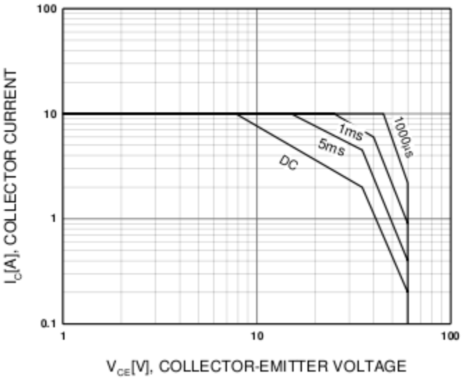


Figure 3. Safe Operating Area

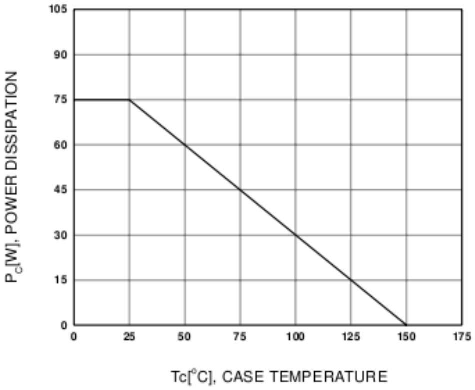


Figure 4. Power Derating