# Physics 364, Fall 2014, Lab #17 **Name:** _____

*(Field Effect Transistors, part I)*

Wednesday, October 29 (section 401); Thursday, October 30 (section 402)

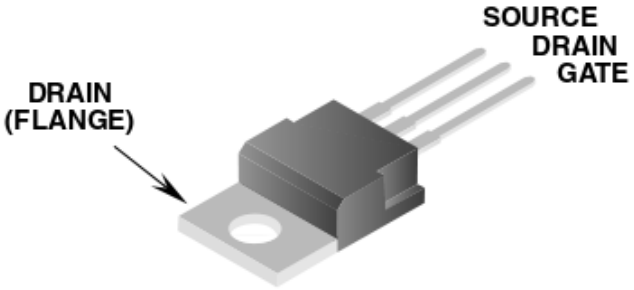
Course materials and schedule are at `positron.hep.upenn.edu/p364`

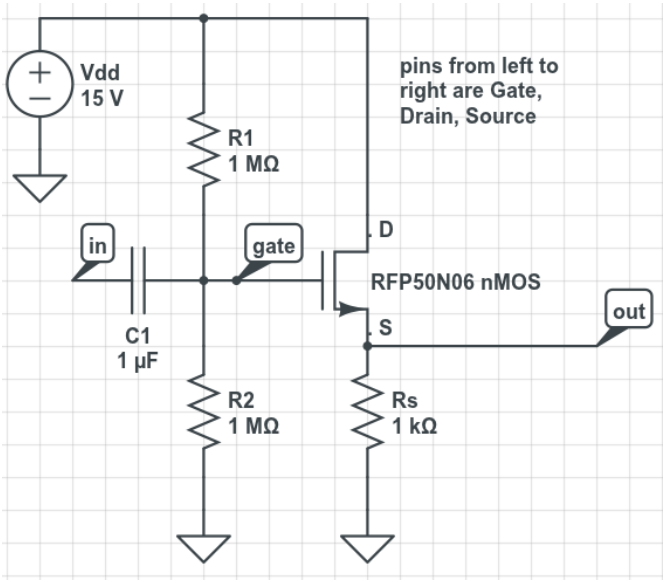
Today's is the first of two labs devoted to Field Effect Transistors. You will see that FETs can be used in many of the same circuits that we are used to building with BJTs.

**Part 1** **Start Time:** _____

**nMOS source follower** (time estimate: 30 minutes)

**1.1** Build the nMOS source follower shown below, using $V_{DD} = +15$ V. A source follower is the FET equivalent of an emitter follower. (Remember that emitter, base, and collector are analogous to source, gate, and drain. Also remember that an $n$-channel MOSFET (a.k.a. nMOS) is the MOSFET analogue of an npn bipolar transistor.) If you like, you can also study and modify this circuit online at `www.circuitlab.com/circuit/2ede5v` .




**1.2** Check that the follower's output actually follows its input.

**1.3** Convince yourself that the FET's input resistance is very large. For example, you might do this by putting a very large (e.g. 1 MΩ) resistor in series with the gate (between the biasing network and the gate) and noticing that there is no detectable voltage drop across it, even when a significant drain current is flowing. Or you might put a micro-ammeter in series with the gate.

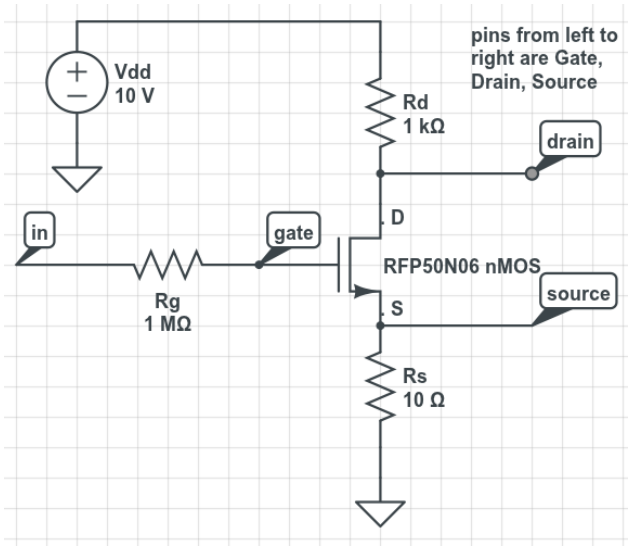
**1.4** By comparing $V_{\text{gate}}$ with $V_{\text{source}}$, see if you can figure out what $V_{\text{threshold}}$ is for this FET: that's the value of $V_{GS}$ at which $I_D$ becomes non-negligible. Check if your value agrees with the data-sheet, found in the back of this handout.

In the next part of the lab, we'll measure some of the characteristics of this MOSFET. You're seeing it work first as a follower so that you can be sure that you're measuring a working FET and that you know which pins are which.

**Part 2** **Start Time:** _____

**n-channel MOSFET characteristics** (time estimate: 45 minutes)

**2.1** Build the circuit shown below, which will allow you to measure the turn-on curve of $I_{DS}$ vs. $V_{GS}$ by analogy with the measurements that you made in Lab 12 of an npn transistor. Use $V_{DD} = +10$ V (though you can try other values, if you like, to vary $V_{DS}$), and drive $V_{\text{in}}$ with a DC output from your function generator.




Measure $V_{\text{gate}}$, $V_{\text{source}}$, and $V_{\text{drain}}$ as you vary $V_{\text{in}}$, and then estimate and graph $I_D$ vs. $V_{GS}$. (Use extra space on next two pages.)

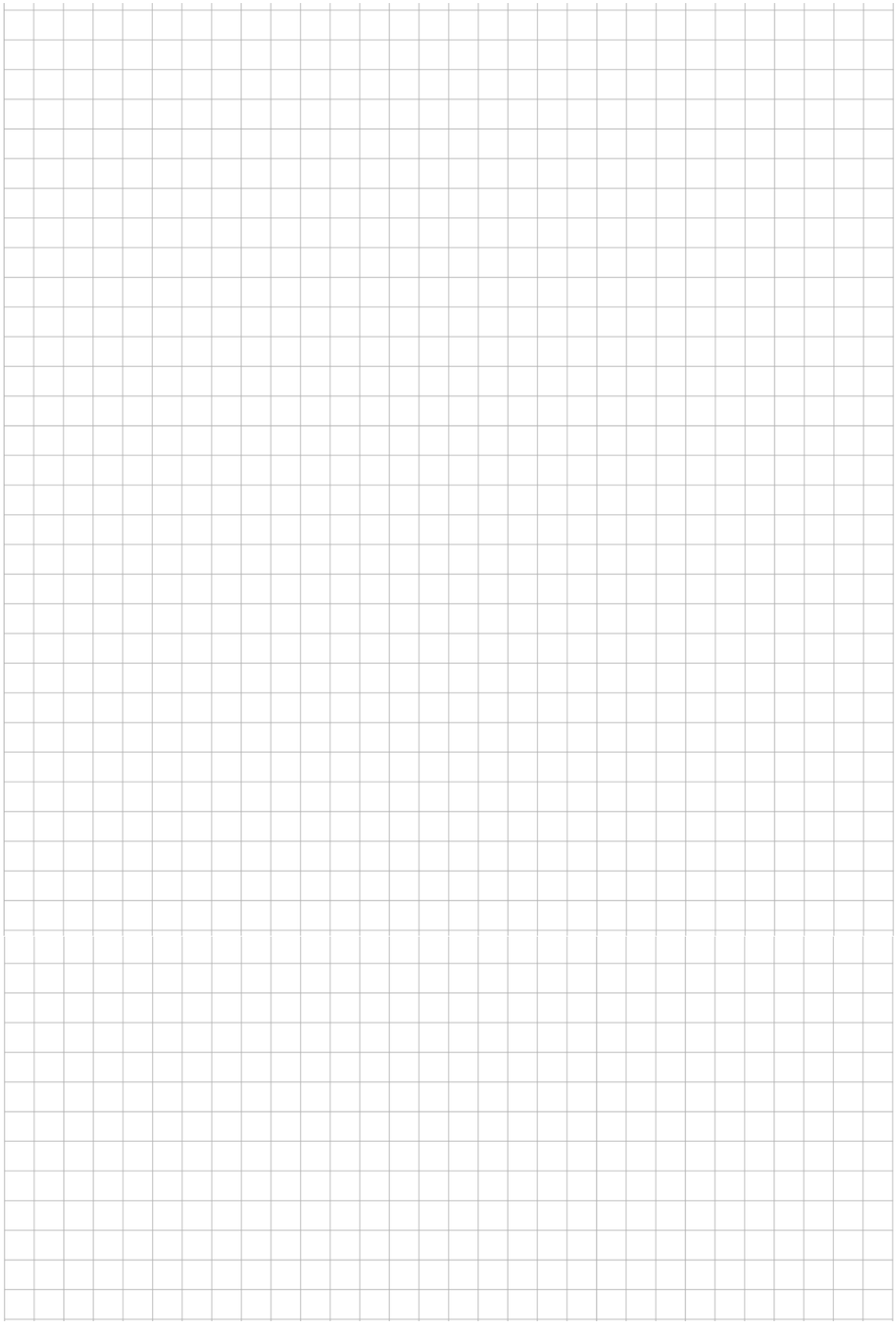
Does the curve look quadratic?

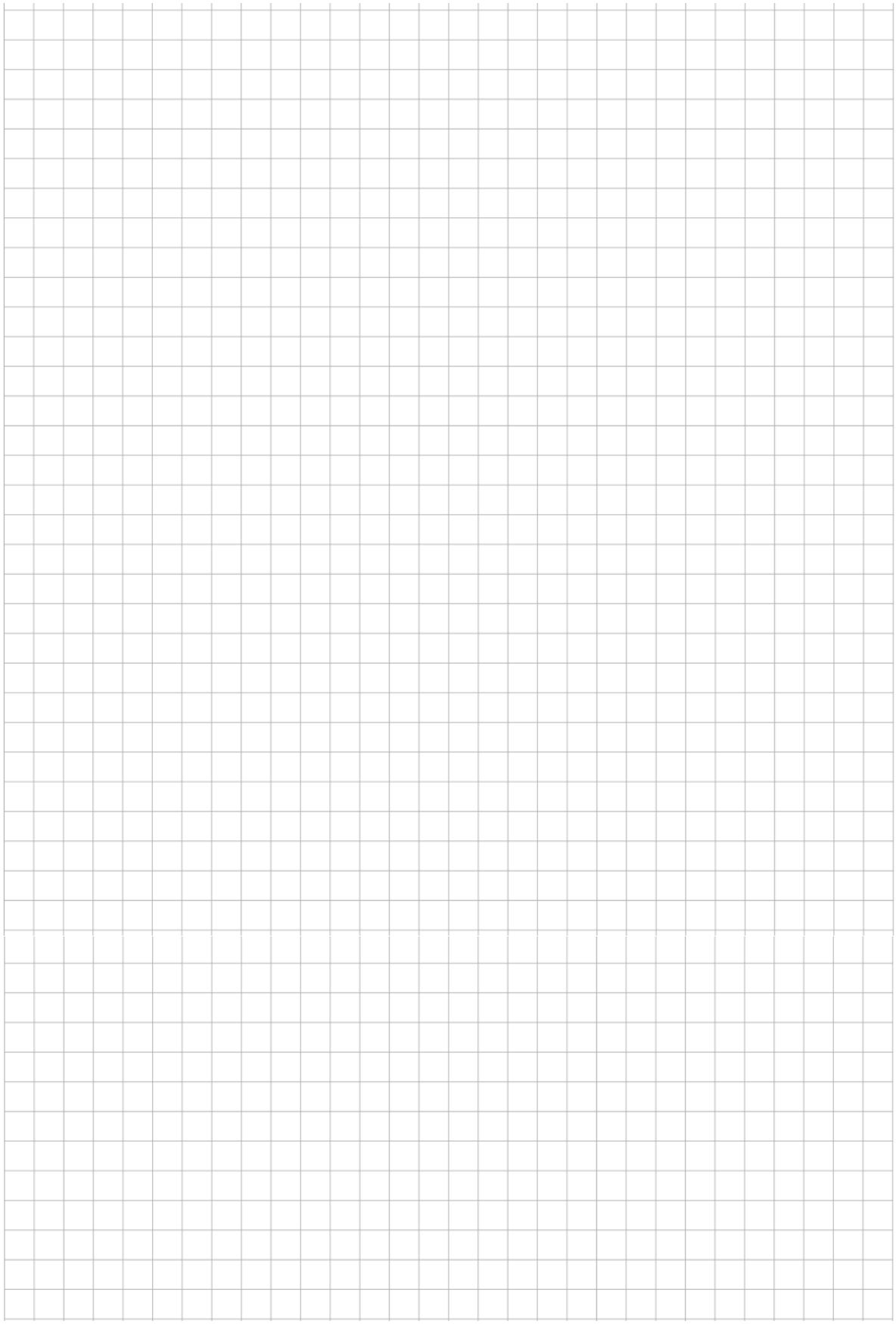
What is $V_{\text{threshold}}$?

What is the constant $K$ for this MOSFET (in units of A/V$^2$)?

Do you see any evidence of gate current?

Remember that $I_D = K \cdot (V_{GS} - V_t)^2$ in active mode. This quadratic rise is in sharp contrast with the exponential rise of $I_C$ vs. $V_{BE}$ for a bipolar transistor. Also, the data sheet lists a wide range for $V_{\text{threshold}}$: anywhere from 2 V to 4 V. This large part-by-part variation is typical of FETs. Online circuit: `www.circuitlab.com/circuit/v5qcgc/` .

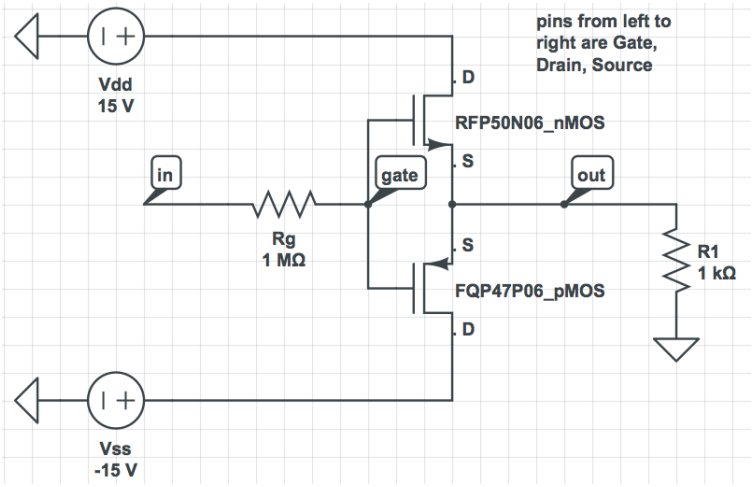




**Part 3** **Start Time:** _____

**CMOS push-pull follower** (time estimate: 45 minutes)

**3.1** Build the CMOS (complementary MOS) push-pull follower shown below, using one nMOS and one pMOS FET. The pins go Gate, Drain, Source from left to right for both the nMOS (RFP50N06) and the pMOS (FQP47P06) FETs. Use $V_{DD} = +15$ V and $V_{SS} = -15$ V. Drive $V_{\text{in}}$ with a sine wave about 8 V in amplitude. Because of the large $V_{\text{threshold}}$, the crossover distortion will be quite noticeable. Looking for a voltage drop across the 1 MΩ resistor, do you see any sign of nonzero gate current? (If the frequency of your input signal is too large, it is possible that you may see evidence of the FET's capacitance.) You can also find this circuit online at `www.circuitlab.com/circuit/kwy7z3/` .




If you wish, you can use a speaker to hear the distortion. If you try this, put a 100 Ω resistor in series with the speaker, at least initially, to limit the power to the speaker. If you like, you can also try the usual opamp-feedback trick to undo the distortion.

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**Part 4** **Start Time:** _____

**Tom's "power MOSFET" exercises** (time estimate: 45 minutes)

Go through as much as you are able, by the end of class, of the "Power MOSFET" exercises from the attached lab by Tom Hayes. There are three sections:

- 12L.1.1 (input impedance),
- 12L.1.2 (switching at higher frequencies), and
- 12L.1.3 (power dissipation: BJT vs. MOSFET). (Use the 8.3 Ω ceramic power resistors, which are rated for 9 W.)

You don't need to write anything down as you work through this last part, but **do make a note of which parts you got through,** and please do call one of us over to share any interesting results you find.

We think you'll especially enjoy, in 12L.1.1, using a MOSFET to turn on/off a light bulb with a miniscule current that flows through your own body!

Use the RFP50N06 n-channel MOSFET that you used in Parts 1–3, as we do not stock the specific MOSFET that Tom's write-up uses.

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# RFP50N06

**Data Sheet** **September 2013**

## N-Channel Power MOSFET 60V, 50A, 22 mΩ

These N-Channel power MOSFETs are manufactured using the MegaFET process. This process, which uses feature sizes approaching those of LSI integrated circuits gives optimum utilization of silicon, resulting in outstanding performance. They were designed for use in applications such as switching regulators, switching converters, motor drivers, and relay drivers. These transistors can be operated directly from integrated circuits.

Formerly developmental type TA49018.

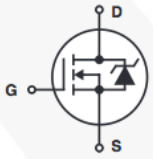
## Ordering Information

| PART NUMBER | PACKAGE | BRAND |
|---|---|---|
| RFP50N06 | TO-220AB | RFP50N06 |

## Features

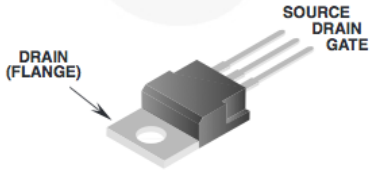
- 50A, 60V
- $r_{DS(ON)} = 0.022\Omega$
- Temperature Compensating PSPICE® Model
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- 175°C Operating Temperature

## Symbol




## Packaging

JEDEC TO-220AB



## Absolute Maximum Ratings $T_C = 25^oC$, Unless Otherwise Specified

| | | RFP50N06 | UNITS |
|---|---|---|---|
| Drain to Source Voltage (Note 1) | $V_{DSS}$ | 60 | V |
| Drain to Gate Voltage ($R_{GS}$ = 20kΩ) (Note 1) | $V_{DGR}$ | 60 | V |
| Gate to Source Voltage | $V_{GS}$ | ±20 | V |
| Continuous Drain Current (Figure 2) | $I_D$ | 50 | A |
| Pulsed Drain Current | $I_{DM}$ | (Figure 5) | |
| Pulsed Avalanche Rating | $E_{AS}$ | (Figure 6) | |
| Power Dissipation | $P_D$ | 131 | W |
| Linear Derating Factor | | 0.877 | W/$^o$C |
| Operating and Storage Temperature | $T_J$, $T_{STG}$ | -55 to 175 | $^o$C |
| Maximum Temperature for Soldering | | | |
| Leads at 0.063in (1.6mm) from Case for 10s | $T_L$ | 300 | $^o$C |
| Package Body for 10s, see Techbrief 334 | $T_{pkg}$ | 260 | $^o$C |

*CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.*

NOTE:

1. $T_J = 25^oC$ to $150^oC$.

## Electrical Specifications $T_C = 25^oC$, Unless Otherwise Specified

| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|---|
| Drain to Source Breakdown Voltage | $BV_{DSS}$ | $I_D$ = 250μA, $V_{GS}$ = 0V (Figure 11) | | 60 | - | - | V |
| Gate to Source Threshold Voltage | $V_{GS(TH)}$ | $V_{GS}$ = $V_{DS}$, $I_D$ = 250μA (Figure 10) | | 2 | - | 4 | V |
| Zero Gate Voltage Drain Current | $I_{DSS}$ | $V_{DS}$ = 60V, $V_{GS}$ = 0V | $T_C = 25^oC$ | - | - | 1 | μA |
| | | | $T_C = 150^oC$ | - | - | 50 | μA |
| Gate to Source Leakage Current | $I_{GSS}$ | $V_{GS}$ = ±20V | | - | - | ±100 | nA |
| Drain to Source On Resistance | $r_{DS(ON)}$ | $I_D$ = 50A, $V_{GS}$ = 10V (Figures 9) | | - | - | 0.022 | Ω |
| Turn-On Time | $t_{ON}$ | $V_{DD}$ = 30V, $I_D$ = 50A, $R_L$ = 0.6Ω, $V_{GS}$ = 10V, $R_{GS}$ = 3.6Ω (Figure 13) | | - | - | 95 | ns |
| Turn-On Delay Time | $t_{d(ON)}$ | | | - | 12 | - | ns |
| Rise Time | $t_r$ | | | - | 55 | - | ns |
| Turn-Off Delay Time | $t_{d(OFF)}$ | | | - | 37 | - | ns |
| Fall Time | $t_f$ | | | - | 13 | - | ns |
| Turn-Off Time | $t_{OFF}$ | | | - | - | 75 | ns |
| Total Gate Charge | $Q_{g(TOT)}$ | $V_{GS}$ = 0 to 20V | $V_{DD}$ = 48V, $I_D$ = 50A, $R_L$ = 0.96Ω, $I_{g(REF)}$ = 1.45mA (Figure 13) | - | 125 | 150 | nC |
| Gate Charge at 10V | $Q_{g(10)}$ | $V_{GS}$ = 0 to 10V | | - | 67 | 80 | nC |
| Threshold Gate Charge | $Q_{g(TH)}$ | $V_{GS}$ = 0 to 2V | | - | 3.7 | 4.5 | nC |
| Input Capacitance | $C_{ISS}$ | $V_{DS}$ = 25V, $V_{GS}$ = 0V, f = 1MHz (Figure 12) | | - | 2020 | - | pF |
| Output Capacitance | $C_{OSS}$ | | | - | 600 | - | pF |
| Reverse Transfer Capacitance | $C_{RSS}$ | | | - | 200 | - | pF |
| Thermal Resistance Junction to Case | $R_{\theta JC}$ | (Figure 3) | | - | - | 1.14 | $^o$C/W |
| Thermal Resistance Junction to Ambient | $R_{\theta JA}$ | TO-220 | | - | - | 62 | $^o$C/W |
| | | - | | - | - | - | - |

## Source to Drain Diode Specifications

| PARAMETER | SYMBOL | TEST CONDITIONS | MIN | TYP | MAX | UNITS |
|---|---|---|---|---|---|---|
| Source to Drain Diode Voltage | $V_{SD}$ | $I_{SD}$ = 50A | - | - | 1.5 | V |
| Reverse Recovery Time | $t_{rr}$ | $I_{SD}$ = 50A, $dI_{SD}/dt$ = 100A/μs | - | - | 125 | ns |