Physics 364, Fall 2014, Lab #18 **Name:** _____

(MOSFET Analog Switches & Digital Intro)

Monday, November 3 (section 401); Tuesday, November 4 (section 402)

Course materials and schedule are at `positron.hep.upenn.edu/p364`

Today, we will first continue our study of Field Effect Transistors by working with a handy MOSFET-based device called an *analog switch*. Then we will briefly begin our study of digital electronics by seeing how a few basic logic gates can be built up out of ordinary mechanical switches. The first three parts of today's lab are borrowed from Tom Hayes's Lab 12, while the last part of today's lab is borrowed from Penn's ESE111.

Note that the first few pages from the data sheets for the DG403 analog switch and LF411 (FET-input) opamp are attached at the end of this write-up, for your reference.

Part 1 **Start Time:** _____

analog switches — intro (mostly from Tom) (time estimate: 15 minutes)

The CMOS analog switch is likely to suggest solutions to problems that would be difficult without it. This lab (the DG403 portions of it) aims to introduce you to this useful device. Schematically, it is extremely simple: it simply passes a signal or does not:

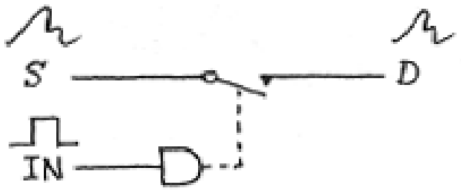


Figure 5: Analog switch: *generic*

The switch we are using has especially nice properties: it is switched by a standard logic signal, 0 V to +5 V. (High, +5 V, is ON.) But it can handle an analog signal anywhere in the range between its supplies, which we will put at ±15 V. It also happens to be a *double-throw* type of switch, nicely suited to selecting between two sources or destinations. Here is the switch, and its pinout:

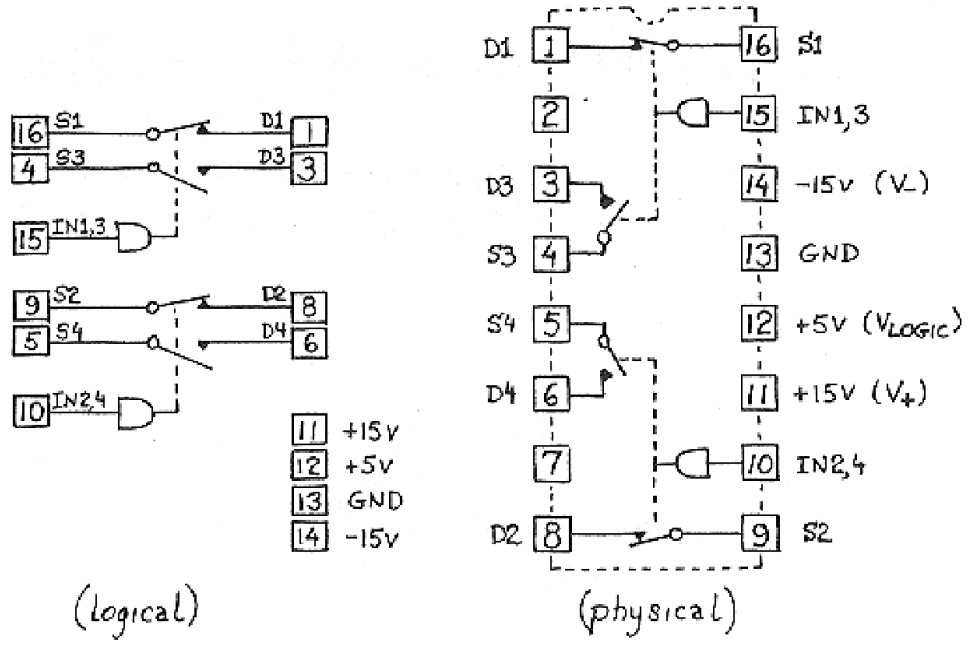


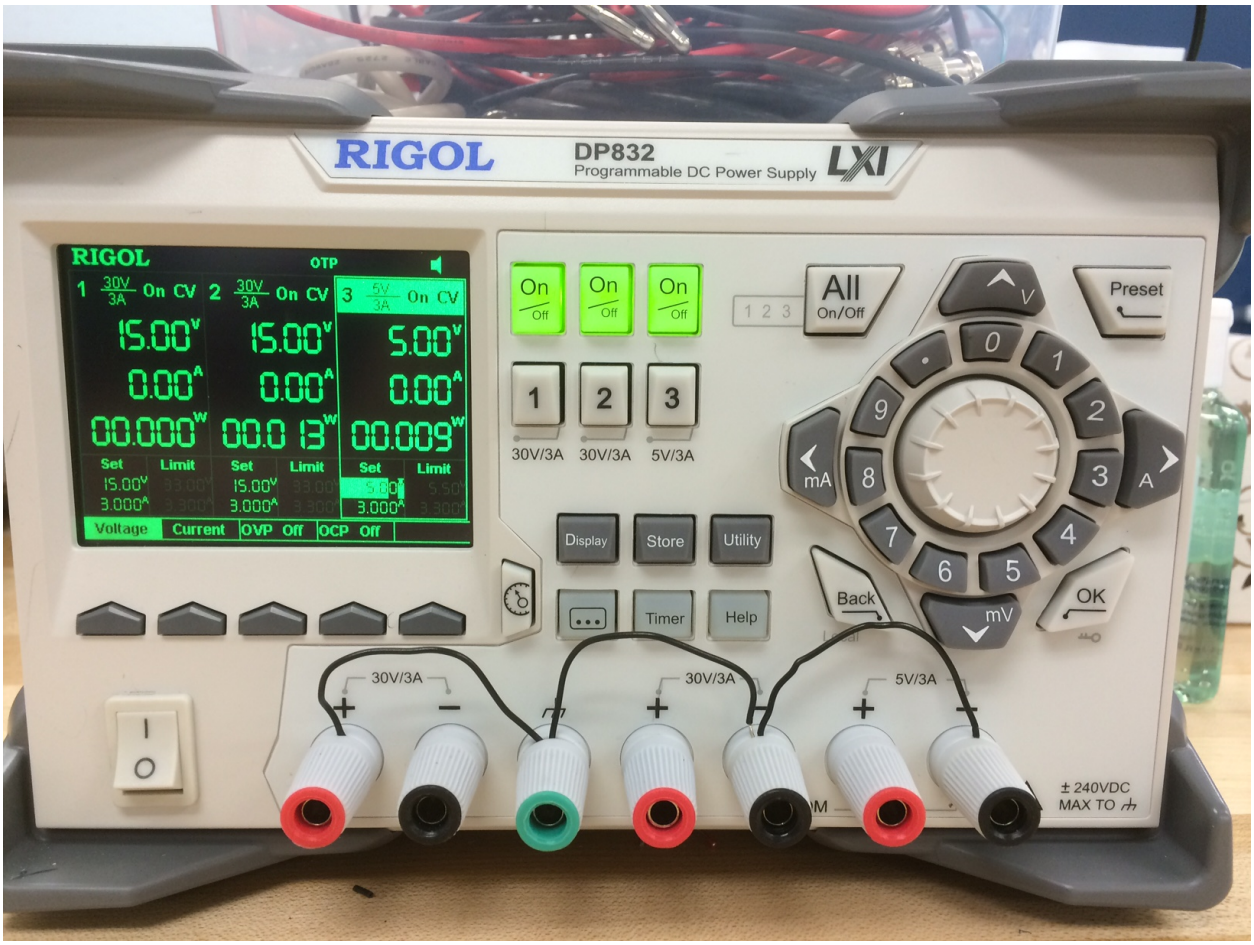
Figure 6: DG403(Maxim) analog switch: block diagram and Pinout

As analog signal source use **Channel 2** of your function generator. As source of the "digital" signal that turns the switch on and off, use **Channel 1** of your function generator. To send a digital "TTL clock" waveform, use a square wave with $V_{\rm pp} = 5$ V and a +2.5 V DC offset. To send a fixed digtal "LOW," use the smallest-possible amplitude (4 $\rm mV_{pp}$) and a 0 V DC offset. (Or just use a wire to ground!) To send a fixed digital "HIGH," use the smallest-possible amplitude and a +5 V DC offset. (Or just use your +5 V power supply rail.) Note

that Channel 1 has a wider range of allowed DC offset values than Channel 2, which is why we're using Channel 1 for the "digital" output.

Caution: Each package contains two analog switches. Tie the unused "IN" terminal to ground or to +5 V. This makes sure the logic input to the switch does not hang up halfway, a condition that can cause excessive heating and damage.

Reminder: The DG403 chip uses **three power supplies:** connect all of them! Using ±15 V and +5 V simultaneously from your three-output power supply will require you to use the first (CH1) power-supply output for −15 V, the second (CH2) power-supply output for +15 V, and the third (CH3) power-supply output for +5 V. Before wiring up your circuit, make sure that all three supplies are properly working for you simultaneously, by measuring each voltage w.r.t. ground. To get this right, it may be helpful for you to connect ground wires as shown by the black wires in the figure.



If you see Tom mention **breadboard "TTL"** for a digital input, in our case that means **Channel 1** of the function generator, set for a 5 V_{pp} square wave with +2.5 V DC offset.

Part 2 **Start Time:** _____

analog switch — imperfections (from Tom) (time estimate: 45 minutes)

We'd like you to see that the switch isn't perfect. Specifically, we ask you to measure its *resistance* when ON and its *feedthrough capacitance* when OFF. But the fun and the main interest of these DG403 analog switches lie in their *applications* (Part 3 of today's lab). So hurry through these preliminary measurements.

2.1 Measuring "on resistance." Ideally, the DG403 analog switch should be a short circuit when it is ON. But in fact, it shows a small resistance, called $R_{\rm on}$. Measure $R_{\rm on}$, using the setup shown below. Use a 1 kHz sine of several volts' amplitude. Confirm that the switch does turn ON and OFF, and measure $R_{\rm on}$.

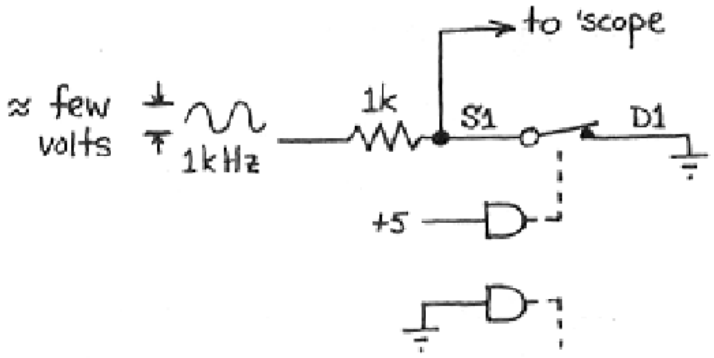


Figure 7: $R_{\rm on}$ **measurement**

2.2 Measuring "feedthrough." The circuit below makes the DG403 analog switch look better: its $R_{\rm on}$ is negligible relative to the 100 kΩ resistor. Confirm this.

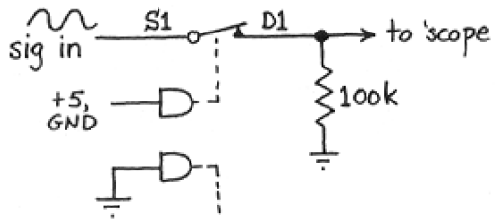


Figure 8: More typical application circuit ($R_{\rm on}$ made negligible)

When the switch is OFF, does the signal pass through the switch? Try a high-frequency sine (e.g. 100 kHz). Try a square wave. If any signal passes through the OFF switch, why does it pass?

Note: as you do the above calculation, don't forget that you are looking at the output with a scope probe whose capacitance (to ground) may be more important than its large $R_{\rm in}$: you're really watching a *capacitive divider* at work. So long as you don't forget this probe capacitance, you should have no trouble calculating the DG403 analog switch's $C_{\rm DS}$.

(Blank page.)

Part 3 **Start Time:** _____

analog switch — applications (from Tom) (time estimate: 90 minutes)

Here's the fun part! If you run out of time before you manage to try all of these circuits, be sure to try the Sample & Hold in any case.

3.1 Chopper circuit. Here is a cheap way to turn a one-channel scope into two channels (or more). Query: what are the limitations on this trick?[1] For a stable display, trigger on one of the input signals, not on the chopper's output, where the transients will confuse your scope. For the "TTL/Sync" input on S3, you can try using the "sync" output from the back of your own function generator, or perhaps more easily, you can just borrow an output from your neighbor's function generator! (Use "utility" to enable the "sync" output, if needed.)

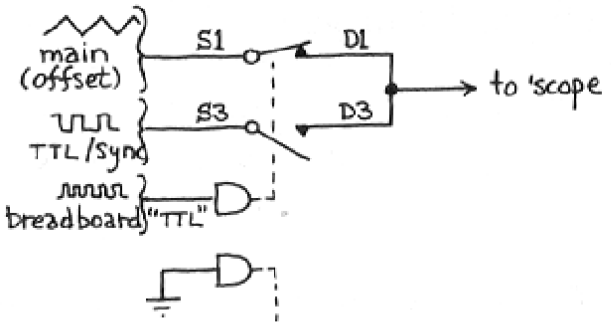


Figure 9: Chopper circuit: displays two signals on one scope channel

[1] The main limitation is speed. This switching scheme will entirely miss a brief transient that occurs while the circuit has chopped to the other input. In addition, R_{on} combined with the scope's capacitance imposes a minimum rise and fall time.

3.2 Sample & Hold. This application is much more important. Is is used to *sample* a changing waveform, *holding* the sampled value while some process occurs. (Typically, this process is a conversion from analog into digital form.) For this circuit, we use the LF411 FET-input opamp. Why is this helpful?

Try the circuit shown below. (Instead of the "manual switch," it's probably easier to use your function generator's Channel 1 square wave, at very low frequency.) Can you infer from the droop of the signal when the switch is in the *hold* position, what leakage paths dominate? (This will be hard, even after some minutes of squinting at the scope screen; don't give your afternoon to this task!)

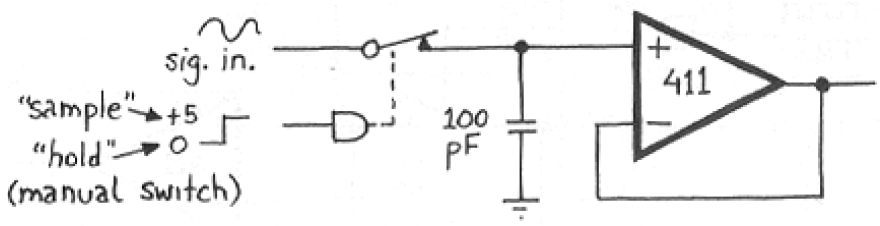


Figure 10: Sample & hold

Query: how does one choose the C value? What good effects, and what bad, would arise from a capacitor choice that was (a) very large; (b) very small?

Can you spot the effect of *charge injection* immediately after a transition on the control input? Compare the specified injection effect and the voltage effect you would predict, given the specification (≤ 60 pC, typical, for the DG403) and the value of your storage capacitor.

Optional: a dynamic view of charge injection

If you inject charge periodically, by turning the switch on and off with a square wave, you can see the voltage error caused by charge injection in vivid form.[2] The *held* voltages ride above the input, by a considerable margin; you will notice the margin varies with the waveform voltage. Why?

Good sample & hold circuits evidently must do better, and they do. See for example the AD582 with charge injection of ≤ 2 pC; and see *The Art of Electronics* §3.3.2.5.

[2]Tom thanks two undergrads for this trick: Wolf Baum and Tom Killian (1988).

3.3 Negative Supply from Positive. ("Flying Capacitor.") You may know that a "switching" voltage regulator can generate a negative output voltage from a positive input voltage, with the help of an inductor. (Students build such a circuit in Tom's course.) For low-current applications the circuit below, which requires no inductors, sometimes is preferable. The trick is to do a little levitation by shoving "ground" about in a sly way. A similar use of "flying capacitors" can generate a voltage larger than the input voltage.

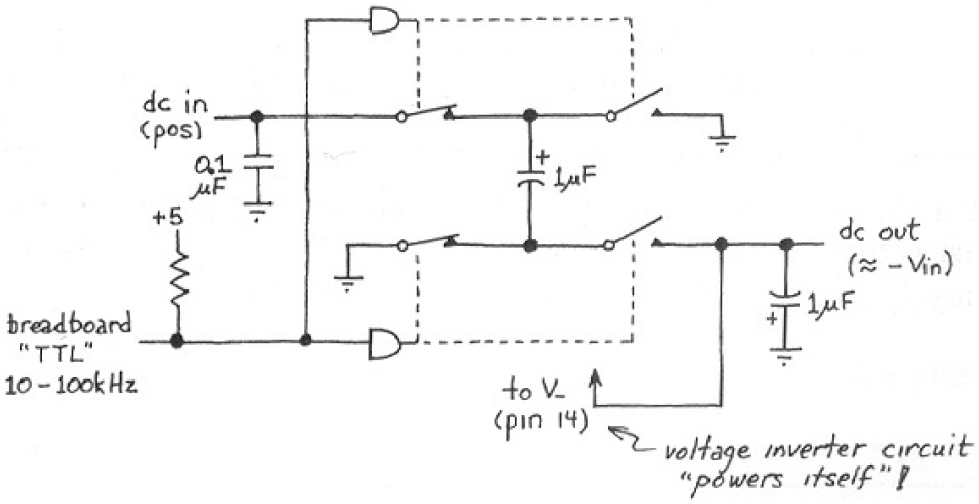


Figure 11: "Flying capacitor" voltage inverter

This circuit provides only a small output current, as you can confirm by loading it.

Such circuits often are put onto an integrated circuit that would otherwise require either a negative supply or a second positive supply, higher than the main supply.[3]

[3]Semiconductor computer memories, for example, sometimes require such a supply. Once upon a time, some memories demanded that the user supply +12 V as well as +5 V. The flying-capacitor trick ended this demand placed on the user; the chip solved the problem internally, and the ICs that lacked the internal step-up were driven out of the market.

3.4 Switched-capacitor Filter. This filter's $f_{3\text{dB}}$ is regulated by the clock rate. This makes it a type convenient for control by computer. In the language of digital filtering, this filter type is a "recursive filter," or an "Infinite Impulse Response" (IIR) filter.

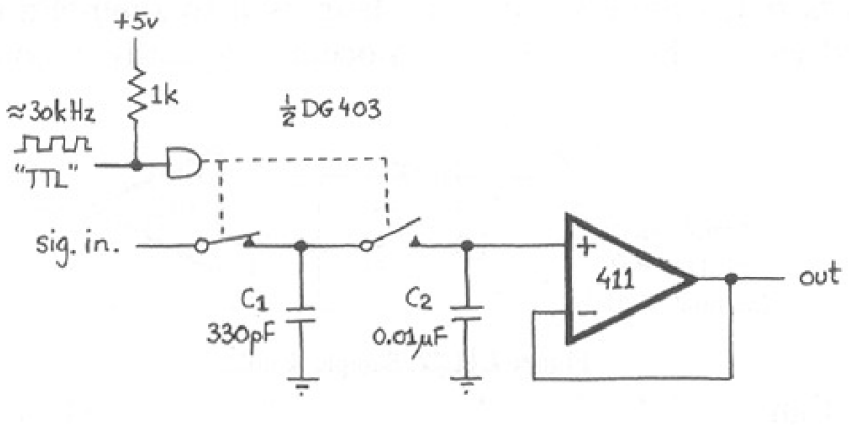


Figure 12: Switched-capacitor low-pass filter

The effective RC simulated by this spoonful-at-a-time charge circuit depends on the relative sizes of the two capacitors (how big the spoon is, relative to the bucket) and on how fast the transfers are made ($f_{\text{switching}}$).

$$f_{3\text{dB}} = \frac{C_1}{C_2} \times \frac{f_{\text{clock}}}{2\pi}$$

Try the circuit, and compare its $f_{3\text{dB}}$ with the predicted value.

Does the filter behave generally like an RC filter? Does it show the same phase shift at $f_{3\text{dB}}$?

Does $f_{3\mathrm{dB}}$ vary as you would expect with clock frequency?

Does the filter fail when the signal frequency is no longer $\ll f_{\mathrm{clock}}$? Because this is a "sampling" filter, you can expect it to get radically confused when the input signal changes quickly relative to the rate at which the square wave transfers samples (the "sampling rate"). This radical confusion is called "aliasing." We'll discuss aliasing later in the context of analog-to-digital conversion; for now, be warned that you should expect trouble when the frequency of a sinusoidal input approaches one-half of the "sampling rate" applied to the analog switch control inputs.

Do you see feedthrough of the clock signal?

(Blank page.)

Part 4 **Start Time:** _____

ESE111 Lab 2, §1–3 (time estimate: 45 minutes)

Go through sections 1, 2, and 3 of the ESE111 Lab 2 (Intro to Digital Logic), included on the following pages. You don't need to write anything down as you go through this last part. The main idea here is to demonstrate to yourself in a very concrete way, using mechanical switches and LEDs, how logic gates work in principle. It then becomes easy to see how MOSFET switches can accomplish the same task.

Note that the first few pages from the data sheets for the DG403 analog switch and LF411 (FET-input) opamp are attached at the end of this write-up, for your reference.